

The 2005 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium will be held in Long Beach, CA on June 11-14, 2005 in conjunction with the IEEE MTT-S International Microwave Symposium. It opens Microwave Week 2005, the largest world-wide RF/Microwave meeting of the year.

The RFIC Symposium brings focus to the technical accomplishments in RF systems, circuit, device and packaging technologies for mobile phones, wireless communication systems, broadband access modems, radar systems and intelligent transport systems.

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Message from the General Chairman

Welcome to the 2005 RFIC Symposium! Again this year, the RFIC Symposium continues to build upon its heritage as one of the foremost IEEE technical conferences dedicated to the latest innovations in RFIC development of wireless and wire line communication IC's, with an exciting technical program. Running in conjunction with the International Microwave Symposium and Exhibit, the RFIC Symposium adds to the excitement of the microwave week with three days focused exclusively on RFIC technology and innovation. The symposium begins on Sunday June 12th with tutorials and workshops focused on RFIC technology, design, and systems.



Joe Staudinger

The RFIC Plenary Session begins at 5:30 pm on Sunday June 12th, following the workshops. It will be held in the Grand Ballroom of the Long Beach Convention Center (LBCC) and opens the formal technical program. Note that the placement of the Plenary Session on Sunday evening at 5:30 pm represents a change in date/time from past years. The Plenary Session will feature two distinguished speakers from industry, Mr. Jerry Neal from RF Micro Devices, and Mr. Ed Healy from Silicon Laboratories. These two renowned guests will share their views on the future direction of semiconductor device technology applied to wireless and mobile communications IC's.

The RFIC reception begins immediately after the plenary, making Sunday evening a highlight of both technical activity and social festivities. This highly attended, enjoyable social event allows attendees to meet with old friends, catch-up on the latest events and interact with professionals in the wireless community.

The technical program continues on Monday and Tuesday with oral paper presentations, panel sessions, and an interactive forum. A panel session during lunch on Monday features a distinguished list of panelists discussing the subject of CMOS displacing GaAs in handset power amplifiers. On Tuesday, a lunch panel session titled, "3G Handsets – Too Much Power in Your Hands?" includes another distinguished set of panelists discussing this high-interest topic. The interactive forum begins on Tuesday afternoon and is an excellent opportunity for attendees to meet authors and discuss their presentations in detail. The RFIC Symposium concludes on Tuesday allowing participants to attend the IMS and ARFTG as well as plenty of time to visit the exhibit hall.

Joseph Staudinger
General Chairman
2005 RFIC Symposium

Message from the Technical Program Committee Chairmen



Luciano Boglione



Stephan Heinen

On behalf of the Technical Program Committee, welcome to the 2005 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. The RFIC Symposium is a leading edge IEEE technical conference dedicated to the advancement of integrated circuits and sub-systems for RF and communications systems. The RFIC Symposium begins on Sunday, June 12th with workshops and tutorials addressing RF technology, design and simulation, at both system and circuit level. The Plenary Session will be held on Sunday evening, right after the workshops. Two leading experts will share their own views during Sunday evening plenary session: Jerry Neal, Co-founder and Vice President, RF Micro Devices, will talk about “Integration Technologies: Cellular and Beyond”; Ed Healy, Vice President of Silicon Laboratories, will discuss “The Drive for Integration”. The RFIC reception will follow the plenary session to allow for everyone to relax and discuss the industry outlook among friends. The regular technical program begins on Monday featuring invited and submitted technical papers. A panel session entitled “CMOS PAs step on the GaAs!” will take place during lunch on Monday and it is posed to allow for many interactive discussions with the audience! Another panel session on Tuesday, “3G Handsets – Too Much Power in Your Hands?”, will have panelists from both industry and academia offer their views on the challenges ahead. The interactive forum on Tuesday afternoon also gives attendees a further opportunity to meet one-on-one with authors. In all, the RFIC Symposium features 25 technical sessions, an interactive forum, 160 presentations, workshops, panel sessions and tutorials. The interest in RFIC technology, and the venue offered by the Symposium to showcase the latest advancements, continues to grow as evidence by a record number of papers submitted to this year’s conference. The 2005 Technical Program Committee keeps working diligently toward the goal of strengthening the technical quality and breadth of the program, to maintain and improve the legacy left by the previous Symposia. This would not be possible without attracting the professional in the field. We would like to thank all the authors for submitting their work to the RFIC conference: this truly exciting program would not be possible without their efforts!

We hope you enjoy the conference.

Stefan Heinen,
Luciano Boglione
RFIC 2005 Technical Program Committee Chairs
IEEE RFIC 2005 Symposium

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RFIC Schedule

The RFIC Symposium will be held in the Long Beach Convention Center (LBCC). The headquarters hotel is the Hyatt Regency which is adjacent to the LBCC. The RFIC Plenary and Reception will be held on Sunday June 12 at the LBCC.

The RFIC Symposium is held in conjunction with the International Microwave Symposium (IMS). Attendees of the RFIC Symposium are invited to attend the IMS Plenary Session on Tuesday June 14 and MTT Social Events.

Saturday June 11, 2005

2:00pm - 6:00pm Registration – LBCC – 104

Sunday June 12, 2005

7:00am - 6:00pm Registration – LBCC – 104

8:00am - 5:00pm Workshops – LBCC

8:00am - 5:00pm Tutorials – LBCC

5:30pm - 7:00pm Plenary –
LBCC – Grand Ballroom

7:00pm - 9:00pm RFIC Reception
LBCC – Grand Ballroom

Monday June 13, 2005

7:00pm - 5:00pm Registration – LBCC – 104

7:00am - 8:00am Speakers Breakfast
LBH Regency E

7:00am - 8:00am Registered Attendee Breakfast
LBCC – 1 Foyer

7:00am - 5:00pm Speakers Preparation
LBCC – 103C

8:00am - 9:40am RFIC Oral Technical Sessions
LBCC – See Listings

9:40am - 10:10am Break – LBCC

10:10am - 11:50am RFIC Oral Technical Sessions
LBCC – See Listings

11:50am - 1:20pm RFIC Panel – LBCC

1:20pm - 3:00pm RFIC Oral Technical Sessions
LBCC – See Listings

RFIC Schedule (Continued)

Monday June 13, 2005 (Continued)

3:00pm - 3:30pm	Break – LBCC
3:30pm - 5:10pm	RFIC Oral Technical Sessions LBCC – See Listings
6:00pm - 8:00pm	Microwave Journal Reception Aquarium of the Pacific

Tuesday June 14, 2005

7:00am - 5:00pm	Registration – LBCC – 104
7:00am - 8:00am	Speakers Breakfast LBCC – LBH Regency E
7:00am - 8:00am	Registered Attendee Breakfast LBH – Foyer – Grand Ballroom
7:00am - 5:00pm	Speakers Preparation LBCC – 103C
8:00am - 9:40am	RFIC Oral Sessions LBCC – See Listings
10:10am - 11:50am	MTT Plenary Session LBCC – Grand Ballroom
11:50am - 1:20pm	RFIC Panel – LBCC
1:20pm - 3:00pm	RFIC Oral Sessions LBCC – See Listings
1:30pm - 3:30pm	RFIC Interactive Forum LBCC – Grand Ballroom
3:30pm - 5:10pm	RFIC Oral Session LBCC – See Listing

Sunday, June 12, 2005 – 5:30 PM

LBCC – Grand Ballroom

Session RSUPL: RFIC Plenary

Session Chair: Joseph Staudinger, Freescale
Semiconductor, Inc.

Session Co-Chairs: Luciano Boglione, Filtronic Sigtek,
Stefan Heinen, RWTH Aachen University

5:30pm Welcome message from General and TPC Chairs,
Announcement of Student Paper Awards

5:45pm Integration Technologies: Cellular and Beyond
Jerry Neal, RF Micro Devices

6:15pm The Drive for Integration
Ed Healy, Silicon Laboratories



Integration Technologies: Cellular and Beyond

**by Jerry Neal
Co-founder and Vice President
RF Micro Devices**

Over the last decade, wireless connectivity has become a way of life. As the world's highest volume consumer electronics product, the cellular phone is a leading driver of mobility. Consumers continue to demand cell phones that feature advanced capabilities, including web access, cameras and even television tuners, which require higher data rates. To accommodate this trend, handset manufacturers are focusing on incorporating these advanced functionalities into the cell phone, and they are looking to their semiconductor suppliers to provide more highly integrated components and complete system solutions that are smaller, better performing and more cost competitive. To drive these higher levels of integration and develop more complex, complete system solutions with optimal performance, RF Micro Devices specializes in using a combination of multiple process and packaging technologies. In addition, RF Micro Devices is honing its radio expertise beyond cellular to provide handset manufacturers multiple radios, including *Bluetooth*[®], wireless LAN and GPS, all of which are forecast to populate cell phones and a proliferation of other wireless devices in the future.

About Jerry D. Neal:

Jerry D. Neal, the company's executive vice president of marketing and strategic development and co-founder, has over 30 years experience in the RF and wireless industry. After obtaining his college education at Gaston Technical Institute and North Carolina State University, Mr. Neal continued his education in the area of computer technology during his employment with Hewlett-Packard. An entrepreneur at heart, Mr. Neal founded Moisture Control Systems, which he later sold to Hancor, Inc. Before co-founding RF Micro Devices, he broadened his exposure to sales and technical business aspects at Analog Devices.



The Drive for Integration:

**by Ed Healy
Vice President
Silicon Laboratories**

As the handset emerges as a platform for the convergence of communications applications, the requirements for smaller, easier-to-implement components are necessary in order to make room for application processors, display requirements and memory chips. Fully-integrated, mixed-signal ICs that offer high performance, flexibility and ease-of-use will continue to dominate the cellular handset market. Monolithic RF ICs in CMOS will enable the technology leap required to meet the challenging integration and cost savings goals of handset manufacturers.

In a market ruled by the consumer, ease-of-use and continuous integration will become increasingly important to handset manufacturers who must deliver cost-effective and differentiated solutions quickly. Best-in-class components allow handset manufacturers to enjoy supply chain control and flexibility as well as faster design cycles. Semiconductor companies that succeed in the cellular market will abandon incremental levels of integration that require multiple discretes, opting rather for revolutionary, first of a kind innovations that push the boundaries of design resulting in integrated, easy-to-use, high performance solutions.

About Ed Healy:

Ed Healy has served as vice president focused on wireless products since 1998. Prior to Silicon Laboratories, Mr. Healy worked as general manager of the Magnetic Storage Division at Crystal Semiconductor/Cirrus Logic. Mr. Healy also held various senior marketing and product planning positions for Zilog, a designer and manufacturer of application specific standard products, and GEC Plessey Semiconductor. Additionally, Mr. Healy was an assistant professor of electrical engineering at the United States Military Academy after serving as an infantry officer. Mr. Healy holds a bachelor's degree in electrical engineering from the United States Military Academy, a master's degree in electrical engineering from Georgia Institute of Technology and a master's degree in management from Stanford University.

Monday June 13, 2005
8:00 AM
LBCC – Room101
Session RM01A: Cellular Transmitters
Chair: Fazal Ali, NOKIA
Co-Chair: Andre Hanke, Infineon

RM01A-1 8:00 AM Invited
A Quad-band 8PSK/GMSK Polar Transceiver

A.W.Hietala, RF Micro Devices

The addition of 8PSK modulation to the GSM standard creates the need for architectural modifications to achieve necessary performance while maintaining a cost effective solution. A large-signal polar modulation transmitter allows the use of an efficient non-linear power amplifier (PA) for both GMSK and 8PSK. Digital interfaces are used for both receiver and transmitter, with analog options available for compatibility with older technology baseband systems.

RM01A-2 8:20 AM Invited
Polar Loop Transmitter for GSM / GPRS / EDGE

T. Sowlati, D. Rozenblit, R. Pulella, M. Damgaard, D. Koh, D. Ripley, E. McCarthy, F. Balteanu, I. Gheorghe, K. Juan, S. Wloczynski, D. Firoiu, Skyworks

A quad band EDGE transmitter using a non-linear GSM type PA is presented. It is based on a Polar Loop architecture that employs separate feedback control of the amplitude and the phase of the output signal. Distortions due to AM-to-PM and AM-to-AM conversion of the non-linear PA are eliminated. No external PA filtering is required to meet the transmitter noise in the receive band. There is no mode change between GMSK and EDGE. The transmitter operates seamlessly in Multi-slot EGPRS.

RM01A-3 8:40 AM**A Highly Integrated CMOS Zero-IF Transmitter for Cellular CDMA Applications**

J. Zhou, W. Sheng, X. Zhang, N. Kim, J. Woolfrey, M. Margarit, S. Vora, C. Persico, Qualcomm Inc.

This first commercially available CMOS CDMA transmitter IC is based on zero-IF architecture and designed for US/China/Korea and Japan cellular bands. The transmitter IC integrates direct upconverter, VGA, driver amplifier, VCO, and both transmit and receive PLLs in 0.24 μ m CMOS. The chip provides 114.9dB power control range and consumes 57.5mA at 2.6V with +6dBm output power and -51.7dBc ACPR.

RM01A-4 9:00 AM**A Digital-to-RF-Amplitude Converter for GSM/GPRS/EDGE in 90-nm Digital CMOS**

P. Cruise, C.-M. Hung, R. B. Staszewski, O. Eliezer, S. Rezek, D. Leipold, and K. Maggio, Wireless Analog Technology Center, Texas Instruments Inc, Dallas, TX 75243

We present the first 90-nm digital CMOS RF power amplifier. This PA contains a large array of NMOS switches, and performs a direct digital-to-RF-amplitude conversion, filtering and buffering in a fully-integrated GSM/EDGE transmitter. Power control is fully digital. 40% efficiency is obtained at 10-dBm output power from 1.4 V and it occupies 0.005 mm².

RM01A-5 9:20 AM**A 1 GHz CMOS Current-Folded Direct Digital RF Quadrature Modulator**

Yijun Zhou, Jiren Yuan, 1. Institute for Infocomm Research, 2. Competence Center for Circuit Design, Department of Electroscience, Lund University

This paper describes a CMOS current-folded direct digital RF quadrature modulator, which uses two 10-bit linear interpolation current steering digital-to-analog converters (DACs) and two current-folded double-balanced mixers. The attenuation of the DAC's image components is significantly increased with linear interpolation, and the reconstruction filter is therefore eliminated. The DAC's baseband differential current signals are fed to the mixer by current-folded structures, which realize the low voltage design and improve the linearity of the modulated RF signal. The chip has been implemented with a 0.35 μ m, double-poly and triple-metal CMOS process.

Monday June 13, 2005
8:00 AM
LBCC – Room102A/102B
Session RM01B: Small Signal LNAs
Chair: Allen Podell, Consultant
Co-Chair: Vijay Nair, Intel Corporation

RM01B-1 8:00 AM
A CMOS 5-GHz Micro-Power LNA

Hsieh-Hung Hsieh and Liang-Hung Lu, National Taiwan University

A fully integrated LNA suitable for ultra-low-voltage and ultra-low-power applications is designed and fabricated in a standard 0.18- μm CMOS technology. With complementary current-reused gain stages, the proposed amplifier exhibits 9.2-dB small-signal gain and 4.5-dB noise figure at 5 GHz while consuming 900- μW dc power from an extremely low supply voltage of 0.6 V. A gain/power quotient of 10.2 dB/mW is achieved in this work.

RM01B-2 8:20 AM
A Sub-mW 960-MHz Ultra-Wideband CMOS LNA

Stanley B. T. Wang, Ali M. Niknejad and Robert W. Brodersen, Berkeley Wireless Research Center, Dept. of EECS, UC Berkeley

This paper presents a sub-mW ultra-wideband (UWB) fully-differential CMOS low-noise amplifier (LNA) operating below 960MHz for sensor network applications. By utilizing both NMOS and PMOS transistors to boost the transconductance, coupling the input signals to the back-gates of the transistors, and combining the common-gate and shunt-feedback topologies, the LNA achieves 13dB of power gain, a 3.6-dB noise figure, -15-dB input match, and -10-dBm of IIP₃ with only 0.72mW of power consumption.

RM01B-3 8:40 AM**A 3-10 GHz Bandwidth Low-Noise and Low-Power Amplifier for Full-Band UWB Communications in 0.25-um SiGe BiCMOS Technology**

N. Shiramizu, T. Masuda, M. Tanabe*, K. Washio, Central Research Laboratory, Hitachi, Ltd., *Renesas Northern Japan Semiconductor Inc.

A SiGe HBT low-noise amplifier (LNA) for UWB systems is presented. In order to reduce the noise figure (NF) over the frequency range from 3 to 10 GHz, a novel LNA structure with an inductor-terminated common-base input stage in front of a resistive-feedback amplifier has been introduced to have increased gain for the input stage and wideband noise matching simultaneously. The LNA in SiGe BiCMOS obtains a wide bandwidth of 14.5 GHz, S₂₁ of 22 dB, and a low NF of 3.9 dB with low power of 13.2 mW.

RM01B-4 9:00 AM**An ESD-Protected, 2.45/5.25-GHz Dual-Band CMOS LNA with Series LC Loads and a 0.5-V Supply**

S. Hyvonen, K. Bhatia*, E. Rosenbaum*, Intel Corp., *University of Illinois at Urbana-Champaign

This ESD-protected, CMOS, Dual-Band 2.45/5.25-GHz LNA consumes only 2.5 mW from a 0.5 V supply, while providing voltage gains of 13.9dB/8.7dB and IIP₃ of +2.9dBm/+3.2dBm (at 2.45GHz/5.25GHz). A dual-band input matching network and series LC resonator loads enable the use of very low supply voltages and simultaneous dual-band operation.

RM01B-5 9:20 AM**18-26 GHz Low-Noise Amplifiers Using 130- and 90-nm Bulk CMOS Technologies**

Shih-Chieh Shin, Szu-Fan Lai, Kun-You Lin, Ming-Da Tsai, Huei Wang, *Chih-Sheng Chang, *Yung-Chih Tsai, National Taiwan University, *Taiwan Semiconductor Manufacturing Company

Two 18-26 GHz CMOS low-noise amplifiers using 130- and 90-nm bulk CMOS technologies are described in this paper. The thin-film microstrip LNA using 130-nm CMOS process demonstrates a peak gain of 12.9 dB at 21 GHz with 3-dB bandwidth of 18.6 to 26.3 GHz and a noise figure of better than 5.4 dB between 20 and 26 GHz. The coplanar waveguide amplifier fabricated by 90-nm CMOS process presents a peak gain of 16.2 dB with a 3-dB bandwidth of 18 to 26 GHz, and a NF of better than 4 dB from 18 to 26 GHz.

Monday June 13, 2005
8:00 AM
LBCC – Room102C
Session RM01C: CMOS RF Device Technology
Chair: Jeffrey Ou, Intel
Co-Chair: Aditya Gupta, Anadigics

RM01C-1 8:00 AM Invited
Scalability of RF CMOS

C. Patrick Yue, S. Simon Wong*, Dept. of Electrical & Computer Engineering, Carnegie-Mellon University; , *Electrical Engineering Dept., Stanford University

The scalability of advanced CMOS processes for RF applications is presented from circuit design and system integration perspective. The impact of transistor scaling and advanced interconnects on active device performance and passive component quality is examined. Key challenges pertaining to high-level integration are assessed including reduced supply headroom and substrate noise coupling. Effective circuit techniques and technology options for overcoming some of these limitations are reviewed. In summary, while many key RF device parameters improve with CMOS scaling, the major setbacks of lower supply voltage and higher mask cost can only be justified for products integrating RF circuits with large baseband digital blocks.

RM01C-2 8:20 AM Invited
RF FET Layout and Modeling for Design Success in RF CMOS Technologies

B. Jagannathan, D. Greenberg, R. Anna, X. Wang, J. Pekarik, M. Breitwisch, M. Erturk, L. Wagner, C. Schnabel, D. Sanderson, and S. Csutak, SRDC, IBM Microelectronics

This paper presents challenges in creating high quality RF FET layouts and models in CMOS technologies spanning 0.25um to 90nm nodes. The focus is on developing a comprehensive methodology to provide robust, high performance parameterized RF FET layout cells and corresponding scalable RF models to enable RF designs that fully leverage the cost benefit potential of CMOS technology.

RM01C-3 8:40 AM**Properties of RF LDMOS with Low Resistive Substrate for Handset Power Applications**

J. Ko, S. Lee, H. Oh, J. Jeong, D. Baek, K. Koh, J. Han*, S.Hong*, I. Son, Samsung Electronics, *KAIST

High performance lateral diffused MOSFET on the CMOS platforms has been developed for the handset power applications. LDMOS with 0.3 μm physical gate length and 7 nm gate oxide shows high f_T and f_{Max} value up to 32 and 26 GHz, respectively as well as low on-resistance of 3.1 $\text{ohm}\cdot\text{mm}$ and high saturated current of about 450 A/m . The breakdown voltage is measured to be 14 V. More than 70 % efficiency at 900 MHz is demonstrated in a unit power cell with the gate width of 1.92 mm.

RM01C-4 9:00 AM**Intermodulation Linearity Characteristics of CMOS Transistors in a 0.13 μm Process**

Guofu Niu, Jun Pan, Xiaoyun Wei, Stewart S. Taylor* and David Sheridan**, Auburn University, *Intel, **IBM

This work presents experimental characterization of intermodulation linearity of CMOS transistors from a 0.13 μm process. The IIP_3 in saturation region is shown to increase with V_{ds} , even though g_m saturates. The IIP_3 in strong inversion is found to be higher than the IIP_3 at the well known linearity sweet spot near the threshold voltage. Longer channel transistors and thick oxide transistors are found to have linearity advantages.

RM01C-5 9:20 AM**Analysis and Modeling of LNA Circuit Reliability**

E. Xiao University of Texas at Arlington

This paper systematically investigates the hot carrier (HC) and soft breakdown (SBD) effects on different low noise amplifier (LNA) circuit configurations. After the MOSFET device RF parameter degradations due to HC and SBD effects are experimentally evaluated, the HC and SBD induced performance degradations of three LNA configurations are evaluated for 0.16 μm CMOS technology. The applications include BlueTooth and WirelessLAN systems. The analytical equations for noise figure are derived, and the degradation models are also obtained. This work can help LNA designers to design more reliable LNA circuits.

Monday June 13, 2005
8:00 AM
LBCC – Room103A/103B
Session RM01D: Wideband Communications
Circuits & Systems

Chair: Jacques C. Rudell, Berkana Wireless
Co-Chair: Albert Wang, Illinois Institute of Technology

RM01D-1 8:00 AM Invited
Integrated TV Tuner Design for Multi-Standard
Terrestrial Reception

Iuri Mehr, Analog Devices, Wilmington, MA

This paper presents issues and trends for monolithic tuner design. It describes the reception requirements and architectures for various standards and channel conditions. Critical block design is addressed with examples from practical implementations. The design is geared toward maximizing the system dynamic range (from -85dBm to +5dBm desired input signal power) and multi-standard functionality. In addition, gearing toward mobile reception, trade-offs to reduce power consumption are discussed.

RM01D-2 8:20 AM
A New Integrated Monocycle Generator and Transmitter
for Ultra-wideband (UWB) Communications

A. Azakkour**, M. Regis*, F. Pourchet*, G. AlquiÈ**, * ACCO S.A, 21 bis rue d'Hennemont, 78100 St-Germain-en-Laye, France., ** LISIF - Université Pierre et Marie Curie, 4 rue Jussieu, 75252 Paris Cedex 05, France.

In this paper we propose a gated pulse generator incorporating two modulation schemes for use in an ultra-wideband impulse radio system. The resulting gated monocycle generator is designed in Jazz Semiconductor Bi-CMOS SiGe technology. Measurements validate the circuit operation over a supply voltage of 2.7V and a power consumption of 243mW. The output monocycles approximate Gaussian monocycles, having pulse duration of 250ps. Proper modulations in time are confirmed.

RM01D-3 8:40 AM**A 3.1-10.6 GHz Ultra-Wideband Pulse-Shaping Mixer**

D. D. Wentzloff, A. P. Chandrakasan, Massachusetts Institute of Technology

This paper presents a mixer for pulse-based ultra-wideband (UWB) communication. Pulses are shaped using a new technique that accurately approximates a Gaussian pulse by exploiting the properties of a BJT. The mixer is fabricated in a 0.18 μ m SiGe BiCMOS process. Simulation and experimental results are presented.

RM01D-4 9:00 AM**A Wide-Band Low-Crosstalk Switch-Matrix and Output Buffer for DVB-S Applications**

T. Copani*, G. Girlando**, S. Smerzi**, A. Castorina**, and G. Palmisano*, *University of Catania, V.le A. Doria 6, Catania, 95125 ITALY, **STMicroelectronics, Str.le Primosole 50, Catania, 95121 ITALY

RF switching blocks play a key role in multi-user broadcast systems. This work investigates the design of a monolithic switch-matrix for dual-user digital-satellite applications in silicon bipolar technology. The circuit performs a 29 dB high isolation between the two output channels and an output 1-dB compression point of +5 dBm. The good overall performance, despite the monolithic approach, is due to the adopted design choices as well as to the proposed output buffer.

RM01D-5 9:20 AM**Design of 24 GHz SiGe HBT Balanced Power Amplifier for System-on-a-Chip Ultra-Wideband Applications**

N. Kinayman, A. Jenkins, D. Helms, R. I. Gresham, M/A-COM, A Tyco Electronics Company

Design of a balanced, three-stage, common-emitter, 24 GHz SiGe HBT power amplifier for ultra-wideband applications is described. The unique features of the amplifier are very flat gain response in the frequency band of interest and sharp gain drop outside of the band, which are important considerations for a system-on-a-chip UWB application. The amplifier has 18 dB nominal gain in the frequency band of 24 GHz \pm 2 GHz. The gain variation is \pm 0.5 dB in the same frequency band. Saturated output power is 12 dBm at 24 GHz.

Monday June 13, 2005

10:10 AM

LBCC – Room101

Session RMO2A: Challenges in RF IC Design

Chair: Stefan Heinen, RWTH Aachen University

Co-Chair: Luciano Boglione, Filtronic Sigtek

RMO2A-1 10:10 AM Invited

RF ICs at Millimeter Waves and Beyond

T. H. Lee, Stanford University

Semiconductors continue to scale impressively, but may never provide sufficient performance for important applications in the terahertz regime. After examining device scaling trends, this talk will review velocity modulation — a concept unfamiliar to many IC engineers, even though devices based on this principle are 70 years old. We will close by presenting recent examples of how combining semiconductor technology with vacuum tube ideas may enable the bridging of the terahertz gap at last.

RMO2A-2 10:30 AM Invited

17 GHz Transceiver Design in 0.13 μ m CMOS

M. Tiebout**, C. Kienmayer*, **, R. Thurninger*, **, C. Sandner**, H.-D. Wohlmuth**, M. Berry**, A.L. Scholtz*, ** INFINOEN Technologies AG,
* Technical University of Vienna

This paper presents the research work towards a fully integrated 17GHz transceiver in 0.13 μ m CMOS. The simultaneous challenge of high-integration, highest frequency and low-voltage design is solved combining optimized on-chip passives and RF circuit techniques with a double-conversion sliding RF-architecture. Three measured chips demonstrate the feasibility of a CMOS transceiver at highest frequency: complete PLL, complete receiver, high-frequency modulator and linear output driver.

RM02A-3 10:50 AM Invited
Challenges in RF Simulation

K. S. Kundert, Cadence Design Systems

RF simulators exploit the nature of RF circuits to overcome bottlenecks that prevent the use of general purpose simulators. While this makes RF simulation possible, it also leads to two significant problems. First, it is difficult to apply RF simulation to larger circuits that are not exclusively RF. Second, it leads to a large number of very specialized analyses, and it is difficult for designers to learn and use the ones they need. Solutions to these two problems are explored in this paper.

RM02A-4 11:10 AM Invited
RF Integrated Feedback Circuits Using On-chip Magnetics

J.R. Long, Electronics Research Laboratory/DIMES, Delft University of Technology

Transistors with gain-bandwidth products exceeding 100GHz are enabling new opportunities for reactive feedback circuits in RFIC applications. This paper outlines the performance advantages of circuits employing on-chip magnetic feedback components. The state-of-the-art in on-chip magnetics for production silicon technologies is reviewed, and RF front-end examples are then presented that demonstrate both wide dynamic range and 1V operation.

RM02A-5 11:30 AM Invited
Redundant MEMS Resonators for Precise Reference Oscillators

E.P. Quevy, R.T. Howe, University of California at Berkeley

This paper describes a new approach for the monolithic integration of precise, temperature-stable reference oscillators for wireless communication. SiGe integrated MEMS technology enables fabrication of an array of resonators, which is key to digital strategies for temperature compensation and trimming of the oscillator's absolute frequency.

Monday June 13, 2005
10:10 AM
LBCC – Room102A/102B
Session RM02B: Advanced VCO Techniques
Chair: Albert Jerng, MIT
Co-Chair: Yann Deval, IXL lab

RM02B-1 10:10 AM

A First RF Digitally-Controlled Oscillator for Mobile Phones

R. B. Staszewski, C.-M. Hung, N. Barton, M.-C. Lee, and D. Leipold,
Wireless Analog Technology Center, Texas Instruments Inc.

We present the first RF digitally-controlled oscillator for cellular phones. It is part of a single-chip GSM transceiver in 90nm CMOS. We derive the effect of high-speed Sigma-Delta varactor dithering on the phase noise. Measured phase noise at 20MHz in SM900 band is -165dBc/Hz and shows no degradation due to the dithering.

RM02B-2 10:30 AM

A Sub-100uW 1.9-GHz CMOS Oscillator Using FBAR Resonator

Y. H. Chee, A. M. Niknejad, J. Rabaey, Berkeley Wireless Research Center,
Dept. of EECS, University of California at Berkeley

This paper presents an ultra-low power CMOS oscillator using Film Bulk Acoustic Resonator (FBAR). The 1.9-GHz oscillator consumes 89 μ W from a 430mV supply and achieves good phase-noise performance of -98 dBc/Hz, -120 dBc/Hz and -138 dBc/Hz at 10kHz, 100kHz and 1MHz offset respectively. This oscillator is implemented in a standard 130nm CMOS process and has the best figure-of-merit compared to other oscillators. To the authors' knowledge, this is the first sub-100 μ W GHz-range oscillator reported.

RM02B-3 10:50 AM**A 26 GHz Coplanar Stripline-based Current Sharing CMOS Oscillator**

H. Krishnaswamy and H. Hashemi, University of Southern California

A coplanar stripline based oscillator topology is introduced that is capable of achieving a low phase noise at extremely high frequencies. This oscillator uses a symmetric current sharing active topology and a high quality factor CPS design in a standard CMOS process without relying on any advanced process features. A 26 GHz prototype, fabricated in a 0.18 μ m CMOS process, achieves a phase noise of -110 dBc/Hz at 1 MHz offset, while drawing a current of 3.36 mA from a 1.8 V supply.

RM02B-4 11:10 AM**A Low Phase Noise 52-GHz Push-Push VCO in 0.18- μ m Bulk CMOS Technologies**

Yi-Hsien Cho, Ming-Da Tsai, Hong-Yeh Chang, Chia-Chi Chang, Huei Wang, National Taiwan University

A V-Band fully integrated complementary push-push VCO is first presented in 0.18- μ m bulk CMOS technologies. In order to lower the phase noise, complementary cross-coupled pairs are used to generate negative conductance. The measured phase noise at 1-MHz offset is about -97 dBc/Hz at 52.6 GHz and is -104 dBc/Hz at 26.3 GHz. To the author's best knowledge, this complementary CMOS VCO achieves the lowest phase noise in comparison with other VCOs using standard bulk CMOS processes in V-Band.

RM02B-5 11:30 AM**A 5 GHz pHEMT Transformer-Coupled VCO**

P.W.Lai, S.I.Long, ECE Department, University of California, Santa Barbara

A transformer-coupled technique is shown to be an area-efficient method for reducing oscillator phase noise. Higher signal amplitude and inductor Q can be achieved without breakdown. A pHEMT process was used to fabricate the 5GHz VCO. The measured phase noise at 3MHz offset frequency is -129 dBc/Hz. The VCO dissipates 9 mW.

Monday June 13, 2005
10:10 AM
LBCC – Room102C
Session RM02C: Active Device Modeling
Chair: Yuhua Cheng, Siliconlinx, Inc.
Co-Chair: Frank Henkel, IMST GmbH, Gemany

RM02C-1 10:10 AM Invited
Next Generation CMOS Compact Models for RF and Microwave Applications

A. M. Niknejad, C. H. Doan, S. Emami, M. Dunga, X. Xi, J. He,
R. Brodersen, C. Hu, Berkeley Wireless Research Center, UC Berkeley, CA

Commercial CMOS chips routinely operate up to 5 GHz and exciting new opportunities exists in higher frequency bands. The BWRC has demonstrated that standard 130nm CMOS technology is capable of operation up to 60 GHz, enabling a host of new mm-wave applications such as Gb/s WLAN and compact radar imaging. This paper will highlight the design and modeling challenges in moving up to these higher frequencies and outline requirements for a next generation RF and microwave compact model.

RM02C-2 10:30 AM
A Lossy Substrate Model for Sub-100nm, Super-100 GHz fT RF CMOS Noise Extraction and Modeling

J. C. Guo, Y. M. Lin, Dept. of Electronics Engineering, National Chiao Tung Univ., Hsinchu, Taiwan

A lossy substrate model is developed to accurately simulate the measured RF noise of 80 nm, super-100 GHz fT nMOSFETs. Substrate RLC network built in the model plays a key role responsible for the nonlinear frequency response of noise in 1~18 GHz regime, which didn't follow the typical thermal noise theory. Good match with the measured S-parameters, Y-parameters, and NFmin before de-embedding proves the lossy substrate model. The intrinsic RF noise can be extracted easily and precisely by the lossy substrate de-embedding using circuit simulation. The accuracy has been justified by good agreement in terms of Id, gm, Y-parameters, and fT under wide range of bias conditions and operating frequencies. The extracted intrinsic NFmin as low as 0.6~0.7dB at 10GHz indicates the advantages of super-100 GHz fT offered by the sub-100nm multi-finger nMOS. The frequency dependence of noise resistance Rn suggests the substrate RC coupling induced excess channel thermal noise apparent in 1~10 GHz regime. The study provides useful guideline for low noise and low power design by using sub-100nm RF CMOS technology.

RM02C-3 10:50 AM**A Large-Signal Model of RF LDMOS with Skin Effects of Power Combining Structures**

J. Han, C. Park, D. Baek*, K. Koh*, J. Ko*, I. Shon*, and S. Hong,
Korea Advanced Institute of Science and Technology(KAIST), *Samsung
Electronics Co., Ltd.

An empirical large signal model is presented to have good accuracy for all the device operating regions up to 20 GHz. Skin effects of combining structures, non-reciprocal capacitance, and non-quasi-static effect are considered in this model. A power transistor of 1.92 mm gate width is modeled and compared with measured data. P1dB of 20 dBm, 19 dB gain and 62 % PAE at P1dB in Pin-Pout properties are exactly predicted by the model.

RM02C-4 11:10 AM**An Improved Silicon RF LDMOSFET Model with a New Extraction Method for Nonlinear Drift Resistance**

K. Lee, J. Yoon, J. Yim, J. Kang, D. Baek*, S. Lee*, I. Shon*, B. Kim, Pohang
University of Science and Technology, *Samsung Electronics Co., LTD

An improved large-signal model of RF LDMOS was developed to enhance the accuracy while maintain the physical meaning. Nonlinear drift resistance was carefully investigated and extracted directly from DC measurement data using the concept of the common intrinsic drain voltage in the two or more LDMOSs with different LDD lengths. The intrinsic part of LDMOS was constructed with the popular BSIM-based model. The model was validated in DC and RF results and had good agreements with measured data.

RM02C-5 11:30 AM**Modeling RF MOSFETs After Electrical Stress Using Low-Noise Microstrip Line Layout**

H. L. Kao¹, Albert Chin^{2,3,*}, J. M. Lai¹, C. F. Lee¹, K. C. Chiang¹,
G. S. Samudra² and S. P. McAlister⁴, ¹ Nano Science Tech. Center,
Dept. of Electronics Eng., Nat'l Chiao-Tung Univ., Univ. System of Taiwan,
Hsinchu, Taiwan, ROC, ² SSDL, Dept. of Elect

A novel microstrip line layout is developed to direct measure the min. noise figure (NF_{min}) accurately instead of the complicated de-embedding procedure in conventional CPW line. Very low NF_{min} of 1.05 dB at 10 GHz is directly measured in 16 gate fingers 0.18 μ m MOSFETs without any de-embedding. Based on the accurate NF_{min} measurement, we have developed the self-consistent DC, S-parameters and NF_{min} model to predict device characteristics after the continuous stress with good accuracy.

Monday June 13, 2005
10:10 AM
LBCC – Room103A/103B
Session RM02D: CMOS Mixers

Chair: Walid Y. Ali-Ahmad, AUB / Maxim
Co-Chair: Sayfe Kiaei, ASU, Connection One

RM02D-1 10:10 AM

A 60-GHz Down-Converting CMOS Single-Gate Mixer

Sohrab Emami, Chinh H. Doan, Ali M. Niknejad, and Robert W. Brodersen, Berkeley Wireless Research Center, Dept. of EECS, University of California, Berkeley

A quadrature balanced single-gate CMOS mixer, designed to exploit the unlicensed band around 60-GHz, is presented. The performance of the fully-integrated mixer fabricated on a standard digital 130-nm CMOS process is given and compared to the simulations. At a radio frequency (RF) of 60 GHz, intermediate frequency (IF) of 2 GHz, and low LO power of 0 dBm, conversion loss is better than 2 dB, and an input-referred 1-dB compression point of ≈ 3.5 dBm was measured.

RM02D-2 10:30 AM

Ultra-Low-Voltage Mixer and VCO in 0.18- μ m CMOS

Hsieh-Hung Hsieh, Kuo-Sheng Chung and Liang-Hung Lu,
National Taiwan University

Using a standard 0.18- μ m CMOS technology, a down-conversion mixer and a voltage-controlled oscillator (VCO) are presented for 5-GHz wireless applications. With a 5.2-GHz RF signal, the mixer has a conversion gain of 3 dB, while the 5.8-GHz VCO exhibits a tuning range of 8.9% and a phase noise of -97 dBc/Hz at 1-MHz offset. Both circuits operate at a reduced supply voltage of 0.6 V. The power consumptions of the mixer and the VCO are 792 and 696 μ W, respectively.

RM02D-3 10:50 AM**A low-IF CMOS Double Quadrature Mixer Exhibiting 58 dB of Image Rejection for Silicon**

M. Notten, J. van Sinderen**, F.Seneschal**, F.Mounaim**, *Philips Research Eindhoven, The Netherlands, **Philips Semiconductors Caen, France

To ease full integration of a TV-receiver a low-IF architecture has been developed. To cancel the adjacent channel at the image of the mixer a quadrature mixer can be used with a limited image rejection of about 40 dB. There for a low-IF passive CMOS double quadrature mixer has been implemented which achieves high dynamic range and more than 58 dB of image rejection over a wide frequency range. The image rejection is now limited by the mismatch in the mixers and the IF filter.

RM02D-4 11:10 AM**A New 0.25- μ m CMOS Doubly Balanced Sub-Harmonic Mixer for 5-GHz ISM Band Direct Conversion Receiver**

Parag Upadhyaya, Mallesh Rajashekharaiyah, Deukhyoun Heo, Yi-Jan Emery Chen, Washington State University, The School of Electrical Engineering and Computer Science, *National Taiwan University, Department of Electrical Engineering

This paper presents a new low power and high IIP2 doubly balanced sub-harmonic mixer for 5 GHz Industrial Scientific Medical (ISM) band direct conversion receiver in a 0.25- μ m CMOS process. The mixer achieves input compression, P1dB, of \approx 8 dBm with conversion gain of 8.2dB while consuming only 1.35 mA current. The mixer also achieves very good IIP2 of 55.3 dBm, IIP3 of \approx 6.5 dBm and an overall double side band noise figure of 5.96 dB. The proposed mixer takes up less than 1mm² including die pads.

RM02D-5 11:30 AM**A Wide-Band Mixer for WCDMA/CDMA2000 in 90nm Digital CMOS Process**

S. Peng, C. C. Chen, A. Bellaouar*, Texas Instruments, *Sirific Corp.

A wide-band mixer with high linearity and insensitive to process and temperature variations, intended for used in WCDMA and CDMA2000 receivers, is implemented in 90nm CMOS process. The measurement data consistently show greater than 7dBm of IIP3 and 50dBm of IIP2 in both low and high frequency bands. In the low frequency band the variation of IIP3 and IIP2 over temperature is merely 0.2 dB and 2.2dB respectively. The current consumption is less than 8mA in the low band and 13mA in the high band.

Monday June 13, 2005

1:20 PM

LBCC – Room101

Session RM03A: WLAN Systems and Architectures

Chair: Derek Shaeffer, Aspendos Communications

Co-Chair: Natalino Camilleri, RFWDS

RM03A-1 1:20 PM Invited

**Circuit Implications of MIMO Technology for Advanced
Wireless Local Area Networks**

W. J. Choi, Q. Sun, J. M. Gilbert, Atheros Communications, Inc.

RM03A-2 1:40 PM

**A 1.4V, 13.5mW, 10/100MHz 6th Order Elliptic
Filter/VGA with DC-Offset Correction in 90nm CMOS**

M. Elmala, B. Carlton, R. Bishop, K. Soumyanath, Communications
Circuits Lab, Intel Corporation, Hillsboro, OR

This paper presents a complete base-band chain for WLAN applications in 1.4V 90nm CMOS. The chain consists of a 6th order elliptic Gm-C 10/100MHz filter and five VGA stages. The design is DC-offset free and uses optimized transconductance for linearity and low-voltage operation. Moreover, the integrators in the filter are compensated for losses through a frequency transformation. The IIP3 is 2dBm @ 13.5dB minimum gain, while dissipating 13.5mW.

RM03A-3 2:00 PM

**Low Power Consumption 2.4 GHz WLAN Front-End
Module for a Multiple Radio Handset**

Chun-Wen Paul Huang, William Vaillancourt, Andrew Parolin, and
Chris Zelle, SiGe Semiconductor, Methuen, Massachusetts, 01844, USA

Abstract – A compact 5 x 6 x 1.4 mm³ 2.4 GHz Wireless LAN (WLAN) front-end module (FEM) is presented. The FEM features low power consumption of 145 mA for 18 dBm output with 3% EVM at 54Mbps transmissions, < -170 dBm/Hz noise emission up to 2 GHz, and high out-of-band interference suppressions, able to support a multi-radio handset with simultaneous operations. The FEM has a 30 dB in-band gain, >24 dB transmit/receive (T/R) isolation under 10:1 mismatch, an integrated regulator, and a temperature compensated power detector. All these unique features provide an easiest integration of a WLAN radio into a multi-radio handset.

RM03A-4 2:20 PM

A Fully Integrated Receiver Front-End Reconfigured by PLL

S.H.Han, C.S.Kim, M.Y.Park, H.K.Yu, Electronics and Telecommunications Research Institute (ETRI)

A 54mW, receiver front-end reconfigured by frequency locking scheme of a PLL is implemented in a 0.18 μ m CMOS technology. The front-end is composed of a discretely tunable low noise amplifier, a down mixer, and a discretely and continuously tunable frequency synthesizer with LC-VCO. The measured performances are 2-2.75GHz tuning range by about 50MHz step, 40dB voltage gain, -25dBm IIP₃, 2.1-2.7dB DSB NF. The synthesizer features a phase noise of -80dBc/Hz at in-band and -120dBc/Hz at 1MHz offset.

RM03A-5 2:40 PM

A 5-GHz Direct-Conversion Receiver with I/Q Phase and Gain Error Calibration

Wei-Zen Chen, Tsorng-Lin Lee, and Tai-You Lu, Integrated Circuits and System Laboratory, Innovative Package Research Center, Department of Electronics Engineering, National Chiao-Tung University

This paper describes the design of a 5GHz direct conversion receiver for WLAN application. Integrated both LNA and mixer in a single chip, the conversion gain of the RF receiver is switch-able to compromise between linearity and noise performance. Gain and phase calibration techniques are proposed to compensate gain and phase error in the I/Q signal paths. By means of this technique, the measured phase error is reduced to be less than 0.6° and gain error less than 0.2 dB. The receiver provides a conversion gain of 28.2 dB in the high gain mode and 11.6 dB in the low gain mode within the signal bandwidth. The overall noise figure (DSB) is 6.4dB in the high gain mode, and the third-order input intercept point (IIP₃) is about -6.8dBm in the low gain mode. Implemented in a 0.18- μ m CMOS technology, the RF receiver consumes 37.4 mW from a 1.8 V supply. Chip area is 1.64 mm².

Monday June 13, 2005

1:20 PM

LBCC – Room102A/102B

**Session RM03B: Frequency Generation Circuits II:
PLLs and Synthesizers**

Chair: Bertan Bakkaloglu, Arizona State University

Co-Chair: Kevin T. Kornegay, Cornell University

RM03B-1 1:20 PM

**A sub-1ps rms-jitter 1-5GHz 0.13 μ m CMOS PLL Using a
Passive Feedforward Loop Filter with Noiseless Resistor
Multiplication**

A. Maxim, M. Gheorghe, Crystal, Austin TX, USA

A sub-1ps rms-jitter multi-GHz PLL was realized in 0.13 μ m CMOS. A fully integrated loop filter was achieved using a passive feed forward architecture that reduces the on-chip capacitance via a noiseless resistor multiplication. The reference spurs are minimized by using a fast switching charge-pump and a reduced reset propagation time phase-frequency-detector. Using high PSRR series and shunt regulators to bias the sensitive PLL building blocks, the supply injected spurs were reduced below -65dBc.

RM03B-2 1:40 PM

**Bandwidth Extension of Low Noise Fractional-N
Synthesizers**

S. E. Meninger, M. H. Perrott, Massachusetts Institute of Technology

This paper examines issues of extending the bandwidth of fractional-N synthesizers. Quantization noise is shown to be the limiting factor in state-of-the-art fractional-N synthesis. A re-framing of the noise model used to analyze synthesizer phase noise leads directly to a methodology to enable high bandwidth synthesis. Measured results of a synthesizer based on the proposed methodology demonstrates >28dB broadband phase noise reduction compared to a state-of-the-art sigma-delta synthesizer.

RMO3B-3 2:00 PM**A Fully Integrated Compact CMOS Fractional Signal Generator for GSM/WCDMA Dual-band Applications**

Y. Park, C.-H. Lee, J. Laskar, Georgia Institute of Technology

We present the new compact low power fractional signal generator based on regenerative division and injection locking for GSM/WCDMA dual-band applications. The design generates $2/3$ of input signal frequency, resulting in DC-offset reduction, phase noise improvement, and the reduced tuning range requirement for a VCO in the direct conversion architecture. The generator is fully integrated ($905\mu\text{m}$ $1012\mu\text{m}$) in a $0.18\mu\text{m}$ standard CMOS process. It generates LO frequency from 1.53GHz to 2.19GHz .

RMO3B-4 2:20 PM**A Fully Integrated GMSK Modulator using BiCMOS Sigma-Delta Frequency Synthesizer with Automatic Loop Gain Calibration**

Chang-Hyeon Lee, Hoon Lee, Pete Good, Skyworks Solutions Inc., 5241 California Ave., M/S:21-2, Irvine, CA 92612, USA

A 2.7V 16mA GMSK modulator using sigma-delta Frequency Synthesizer with automatic loop gain calibration is implemented on a 3.2mm^2 die area using $0.35\mu\text{m}$ BiCMOS process. It meets GSM transmit spectral mask spec. and achieves a close-in phase noise of $-90\text{dBc}/\text{Hz}$ and spurious noise level of $-75\text{dBc}/\text{Hz}$ without modulation.

Monday June 13, 2005

1:20 PM

LBCC – Room102C

Session RM03C: Front-End Design Techniques

Chair: Sudipto Chakraborty, Texas Instruments, Inc

Co-Chair: Kirk Ashby, Microtune, Inc

RM03C-1

1:20 PM

Invited

Circuit Techniques for CMOS Multiple-Antenna Transceivers

D.J. Allstot*, S. Aniruddhan*, G. Banerjee**, M. Chu*, X. Li***, J. Paramesh**, S. Shekhar* and K. Soumyanath**, *Univ. of Washington, **Intel Corp., ***QualComm Corp.

Circuit techniques in multiple-antenna systems reduce die area and power, and maintain state-of-the-art performance. Device desensitization techniques achieve simultaneous noise and input matches in LNA circuits. A transformer coupled common-gate LNA achieves low noise figure and power, and a Colpitts voltage-controlled oscillator topology provides robust start-up and maintains excellent phase-noise. Finally, a cartesian combining method is applied to the design of multiple-antenna transceivers.

RM03C-2

1:40 PM

An Integrated LMS Adaptive Filter of TX Leakage for CDMA Receiver Front Ends

V. Aparin, G. Ballantyne, C. Persico, A. Cicalini, QUALCOMM Inc.

The theory and practical implementation of an adaptive filter of the TX leakage in CDMA receivers are described. The filter was designed as part of a 0.25um CMOS cellular-band receiver. It achieved the maximum rejection of the TX leakage of 28-30dB which was limited by the reference signal leakage to the LNA output. The LNA NF and gain degraded by 1.3dB and 1.7dB respectively after adding the filter.

RM03C-3

2:00 PM

Experimental Results at One GHz on Linearizing an NMOS Transistor with a Parallel PMOS Transistor

T. P. Weldon, D. T. Lieu, M. J. Davis, University of North Carolina at Charlotte

A simple circuit consisting of an nMOS transistor in parallel with a pMOS transistor is shown to reduce nonlinear distortion. Measured experimental results show more than 10 dB reduction in third order distortion at 1 GHz for a prototype 0.18 micron CMO integrated circuit. Experimental data further suggest that the relative increase in third order output intercept point greatly exceeds the corresponding increase in power supply current. Since the proposed circuit is itself a three-terminal device, it can also be used as a building block for larger circuits. Finally, theoretical linearization conditions are presented in terms of the gains and intercept points of the nMOS and pMOS devices.

RM03C-4

RM03C-4 – WITHDRAWN

RM03C-5 2:40 PM

Using Auxiliary Amplifier to Cancel Third-Order Intermodulation Distortion For A 1.9 GHz CMOS Linear Amplifier Design

Kung-Hao Liang, Chien-Chih Ho, Meng-Wei Hsieh and Yi-Jen Chan,
Department of Electrical Engineering, National Central University

A new linearization method of microwave amplifier design by canceling the third-order intermodulation component ($2f_2-f_1$) is proposed. The main amplifier is combined with an auxiliary amplifier, which is appropriately designed by the gain and bias conditions. The output frequency spectra of the main amplifier are subtracted by this auxiliary amplifier. The third-order distortion will be canceled since these two amplifiers are designed by a differential-pair stage. IIP₃ improvement as large as 11 dB has been obtained, where this amplifier achieves a 11.5 dB gain at 1.9 GHz, fabricated by using 0.18 μm CMOS technologies. The circuit consumed 11.5 mA or 11 mA based on the condition of auxiliary amplifier on or off, respectively. The auxiliary amplifier consumes small than 0.8 mW dc power and causes only 0.2 dB gain reduction of the main amplifier.

Monday June 13, 2005

1:20 PM

LBCC – Room103A/103B

Session RM03D: Efficiency Improvement Topologies

Chair: Tina Quach, Freescale, Inc.

Co-Chair: David Ngo, RF Micro Devices, Inc.

RM03D-1 1:20 PM

A 20mA Quiescent Current 40% PAE WCDMA HBT Power Amplifier Module with Reduced Current Consumption Under Backoff Power Operation

G. Hau, S. Caron, J. Turpel, B. MacDonald, Fairchild Semiconductor Corp.

A 1.95GHz WCDMA HBT power amplifier module (PAM) with reduced backoff power current consumption is presented. Improved efficiency is obtained by switching the final stage of the PA between two transistor cells, which are terminated with different load impedance. The PAM is biased at quiescent current of 20mA, and exhibits 40% PAE and -40dBc ACLR1 at 28dBm Pout. At backoff Pout of 17dBm, it achieves 16% PAE which represents 40% reduction in current consumption compared to conventional design.

RM03D-2 1:40 PM

A SiGe PA with Dual Dynamic Bias Control and Memoryless Digital Predistortion for WCDMA Handset Applications

J. Deng, P.S. Gudem, L.E. Larson, D. Kimball and P.M. Asbeck, Center for Wireless Communications, Dept of ECE, University of California at San Diego

This paper demonstrates a two-stage 1.95GHz WCDMA handset PA implemented in 1.8mm² in a 250nm SiGe BiCMOS process. With an integrated dual dynamic bias control in the output stage, the average power efficiency of the two-stage PA is improved by over a factor of two. An off-chip memoryless digital predistortion is also adopted to improve the linearity of the power amplifier, satisfying the 3GPP WCDMA ACPR specifications with 26dBm average channel output power and a peak PAE of 27%.

RM03D-3 2:00 PM**Linear RF CMOS Power Amplifier with Improved Efficiency and Linearity in Wide Power Levels**

N. Srirattana, P. Sen, H.-M. Park*, C.-H. Lee, P. E. Allen, and J. Laskar, Georgia Institute of Technology, *Maxim Integrated Circuits

The design of RF CMOS power amplifier using large and small transistors in parallel at the output stage for efficiency and linearity enhancement is proposed in this paper. A small transistor is used for low power amplification where a larger transistor is turned off to reduce DC power consumption and increase efficiency in back-off region. The technique to improve the linearity of FET amplifiers by offsetting the gate biases to cancel the nonlinearity products is implemented additionally.

RM03D-4 2:20 PM**A Single-chip Variable Supply Voltage Power Amplifier**

I. A. Rippke, J. S. Duster*, K. T. Kornegay*, Xpedion Design Systems, Inc., *Cornell University

A single-chip implementation of a variable supply voltage power amplifier (PA) is presented. The circuit is design in SiGe BiCMOS technology and is composed of a differential power amplifier designed for WCDMA operation and a "buck" DC-DC converter. The combined system varies the supply voltage of the PA from 2.7V to 1.2V and maintains system linearity while the output power is not at its maximum. The system achieves an average efficiency improvement of 46% over a fixed supply system.

RM03D-5 2:40**A New Series-Type Doherty Amplifier for Miniaturization**

J. Jung, U. Kim, J. Jeon, J. Kim, K. Kang*, Y. Kwon, Seoul National University, *Wavics co., Ltd.

A new topology of Doherty amplifier is proposed to reduce the circuit size by eliminating the bulky 3dB 90° hybrid coupler. Unlike the classical Doherty amplifier, the carrier and peak amplifiers are connected in series together with an impedance-inverting network. A simple matching circuit between the peak and carrier amplifier replaces the input hybrid coupler. In this way, the need for an input hybrid coupler is eliminated, facilitating integration and miniaturization.

Monday June 13, 2005

3:30 PM

LBCC – Room101

**Session RM04A: RF Transceivers for
2G & 3G systems**

Chair: Madhukar Reddy, MaxLinear Inc.

Co-Chair: Didier Belot, ST Microelectronics

RM04A-1 3:30 PM Invited

Digital RF CMOS Transceivers for GPRS and EDGE

Christian Munker, Bernd-Ulrich Klepser, Burkhard Neurauter*,
Christian Mayer*, Infineon Technologies, *DICE GmbH & Co KG

A GPRS solution using sigma-delta modulation and an EDGE solution using digital polar modulation are presented. The single-chip, quad-band transceivers have been implemented in a 0.13 μ m CMOS technology. The lock-in time of the sigma-delta modulator with integrated loop filter is less than 120 μ s with a phase error of 1.2 ∞ rms and an output power of 3.5 dBm; it is fully compliant to the GSM specification. The EDGE transceiver shows a nominal margin of 11 dB to the critical 400 kHz specification.

RM04A-2 3:50 PM

**A Fully Integrated Inter-Stage-Bandpass-Filter-Less
Direct-Conversion Receiver for W-CDMA**

M. Tamura, T. Nakayama, Y. Hino, A. Yoshizawa, and K. Takagi,
Sony Ericsson Mobile Communications Japan, Inc.

A W-CDMA direct-conversion receiver (RX) with an LNA has been implemented as a part of transceiver using a 0.35- μ m SiGe BiCMOS technology. The RF bandpass filter between the LNA and mixer has been eliminated without putting excessive demands on the duplexer. The target IIP2 was derived with the HPSK TX signal in mind. Measurement showed that the IIP2 is at least +36.8 dBm, and the NF is 5.7 dB. The RX draws 31mA from the 2.7 V supply. The transceiver is fully compliant with 3GPP/FDD standards.

RM04A-3 4:10 PM

**Compact Radio System Module for Triple-band GSM
Cellular Phones**

H. Okabe, T. Ido, T. Endo*, Hitachi, Ltd., *Renesas Technology Corp.

A compact radio system module, 10x10.3x1.2 mm³, for triple-band GSM cellular phones is presented. The module was miniaturized by employing a simple front-end architecture, highly integrated transceiver IC, one chip HPA-MMIC, and thin four-layer laminate substrate. Design considerations for a very compact radio system module, i.e., techniques for avoiding thermal and electrical interaction, are discussed. The excellent performance of the developed module is demonstrated.

RM04A-4 4:30 PM**A 1.9GHz SiGe BiCMOS PHS Transceiver with an Integrated PA and a Fast Settling PLL**

M. A. I. Mostafa, C. K. Quek, A. E. Moznine, W. Roberts, M. Romney, D. Walker, D. Stegmeir, K. Tran, N. King, S. Farahvash, and R. Koupal, Micro Linear Corp.,

A fully integrated PHS transceiver achieving 105dBm sensitivity and +21dBm output power is implemented in a 0.35 μ m SiGe BiCMOS process occupying an area of 13 mm² and dissipating 74mA in RX mode and 280mA in TX from 3V supply. The receiver does not require any external filters. The TX integrates a linear +21dBm PA and achieves 5% EVM and 60dBc ACP. The transceiver integrates a fractional-N synthesizer with <30 μ s lock time and -120dBc/Hz phase noise @ 600kHz offset frequency.

RM04A-5 4:50 PM Invited**A Tri-band (2100/1900/800 MHz) Single-chip Cellular Transceiver for WCDMA/HSDPA**

D. Kaczman, C. Dozier, N. Godambe, H. Guimaraes, M. Shah, M. Rachedine, M. Alam, L. Han, W. Shepherd, D. Cashen, J. Ganger, K. Coughlar, B. Getka, E. Brotkowski, Freescale Semiconductor

The RFIC implemented is a tri-band (2100/1900/800 MHz) direct conversion transceiver for 3G cellular applications supporting WCDMA and HSDPA (High Speed Downlink Packet Access) schemes. It was implemented using an enhanced CDR1 BiCMOS (0.35 μ) SiGe:C process with electroplated Copper inductors. The zero-IF receiver is comprised of three sets of quadrature mixers, 7th order baseband filtering and dc offset correction circuitry. The direct launch transmitter is made of a 3rd order baseband filter, an I/Q modulator with variable gain, an RF variable gain amplifier, and a PA driver. There are two on-chip process tracking oscillators to tune the filter poles and zeros. There are two fractional-N synthesizers together with two automatically calibrated integrated VCOs on the die. The IC draws 34 mA in receive and 49-64 mA in transmit using a 2.775V supply voltage.

Monday June 13, 2005

3:30 PM

LBCC – Room102A/102B

**Session RM04B: Passive Modeling, De-embedding
and Design Methodology**

Chair: Kevin McCarthy, University College Cork, Ireland

Co-Chair: Patrick Yue, Carnegie Mellon University

RM04B-1 3:30 PM Invited

Analog RF Model Development With Verilog-A

B. Troyanovsky, P. O'Halloran, M. Mierzwinski, Tiburon Design Automation

Over the past several years, analog hardware description languages (AHDLS) have gained increasing acceptance in the areas of analog and RF circuit simulation. The widespread adoption of these standardized languages promises to bring substantial benefits to both analog model developers and to the users of analog simulation tools. In this paper, we examine the applicability of the Verilog-A hardware description language for analog RF modeling tasks.

RM04B-2 3:50 PM

**Characterization, Design, Modeling, and Model
Validation of Silicon on-Wafer M:N Balun Components
under Matched and Un-Matched Conditions**

F. Rotella, G. Tkachenko, Y. Cheng, Skyworks Solutions

In this paper, we characterize and model M:N baluns for RFIC design. A modeling methodology is presented based on a scalable lumped-element approach that incorporates both skin effect and substrate loss. The impedance transformation characteristics of the scalable model are explored. The modeling approach is validated with measured S-parameters and extracted impedances from various circuit configurations. Matching considerations are addressed by evaluating the model accuracy with measured data under matched and un-matched conditions.

RM04B-3 4:10 PM

**Modeling Methodology of Integrated Five-Port Balun
Using Two-Port RF Measurement**

Kai-Ye Huang, Chia-Jen Hsu and Len-Yi Leu, Winbond Electronics Corp.

A comprehensive investigation of modeling methodology for integrated balun fabricated by 0.18 μ m, mixed signal process are presented. We proposed an improved lumped-element circuit and a three-step method to characterize and model the five-port balun by using two-port RF measurement. The frequency dependence of inductance and resistance is considered in the lumped-element model. Both inverting and non-inverting configuration were examined to enhance the model accuracy.

RM04B-4 4:30 PM**A Decomposition and Reconstruction Scheme for Broadband Modeling of On-Chip Passive Components Using Modified T-Equivalent Circuit**

T.S. Horng, J.K. Jau, Y.S. Tsai, and C.S. Huang, Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan

This paper presents the state-of-the-art technique for broadband modeling of on-chip passive components. The proposed decomposition and reconstruction methodology can efficiently and accurately establish the broadband SPICE model for an arbitrary multi-port reciprocal component over an extremely large bandwidth. The idea is to decompose a multi-port network into a number of one-port networks which can be lumped modeled simply and easily. Then a reconstruction process based on the modified T-equivalent circuit topology is invented to combine these one-port lumped models into a broadband multi-port model. In this modeling study, the S parameters for a series of passive components including spiral inductors, MIM capacitors, bifilar transformers and baluns fabricated using 0.18 μm RF-CMOS foundry process have been measured up to 20 GHz. The modeled S parameters agree quite satisfactorily with the measured results over the entire measurement frequency range.

RM04B-5 4:50 PM**A Fully-Scalable De-Embedding Method for On-Wafer S-Parameter Characterization of CMOS RF/Microwave Devices**

M. H. Cho, C. S. Chiu, G. W. Huang, Y. M. Teng, L. H. Chang, K. M. Chen, National Nano Device Laboratories

A scalable de-embedding method for on-wafer device measurements is presented. This method is based on transmission-line theory and does not require any equivalent-circuit model for external parasitics. Compared with the conventional scalable de-embedding method, the proposed procedure can further eliminate the unwanted parasitics from the source terminal. The performance of this new method was also validated by comparison with the “open-short” de-embedding technique.

Monday June 13, 2005
3:30 PM
LBCC – Room102C
Session RM04C: Optical System ICs and Architectures

Chair: Louis Liu, Northrop Grumman
Co-Chair: Kursad Kiziloglu, Intel Corp.

RM04C-1 3:30 PM

1V, 10mW, 10Gb/s CMOS Optical Receiver Front-End

Drew Guckenberger, Jeremy D. Schaub*, Daniel Kucharski, Kevin T. Kornegay, Cornell University, *IBM Austin Research Laboratory.

A 1V, 10mW CMOS optical receiver front-end is presented that achieves 10Gb/s operation. The linear gain is 65.6dB (1.9k?) and the optical sensitivity is -13.1dBm for a BER of 1e-12. The receiver is implemented in a 0.12 μ m digital CMOS process with a core size of 175 μ m x 250 μ m.

RM04C-2 3:50 PM

A 3.3V 10Gb/s SiGe Limiting Transimpedance Amplifier Using a Pseudo-Differential Input and a Limiting Cherry-Hooper Stage

A. Maxim., Maxim Integrated Products, Fiber Communications Division, Austin, TX

A 10Gb/s limiting transimpedance amplifier was realized in a 0.2 μ m $f_T=60$ GHz SiGe technology. A pseudo-differential common-emitter input stage with capacitive and input bondwire inductive peaking was used. The input capacitance of the linear Cherry-Hooper stage is reduced through a neutralization technique that ensures a low voltage operation due to the elimination of the inter-stage emitter followers. The limiting amplifier uses a reduced noise sensitivity cross-coupled Cherry-Hooper architecture.

RM04C-3 4:10 PM

Low Power Consumption 10-Gb/s SiGe Modulator Drivers with 9Vpp Differential Output Swing Using Intrinsic Collector-Base Capacitance

Day-Wei Li, Li-Ren Huang, Chia-Ming Tsai, SoC Technology Center, Industrial Technology Research Institute, Hsinchu 310, Taiwan, R.O.C.

A novel intrinsic collector-base capacitance feedback network is incorporated into the conventional cascode circuit configuration to implement a 10-Gb/s modulator driver in 0.35 μ m SiGe BiCMOS technology. The driver could output 9Vpp differential output swing with edge speed less than 29ps while it consumes power as low as 0.8W. The proposed driver consumes the lowest power and occupies the smallest die area, and outputs the highest swing than the ever-reported silicon-based modulator drivers.

RM04C-4 4:30 PM**High Voltage Swing and High Data Rate Multiplexers in SiGe Technology**

Martin Wurzer, Herbert Knapp, Thomas F. Meister, Infineon Technologies AG

A 2:1 time-division multiplexer with high differential output voltage swing of $2 \times 2 V_{pp}$ operating at a data rate of 40 Gb/s is reported. The shows rise and fall times of about 11 ps and consumes 1.65 W. It is fabricated in a $0.35 \mu\text{m}/200\text{GHz-ft}$ production near SiGe bipolar technology with a V_{CE0} of 1.8V. Furthermore a high-speed 2:1 multiplexer capable of processing data rates higher than 80 Gb/s has been realized in the same technology. It consumes 0.75 W.

RM04C-5 4:50 PM**An 80-Gb/s 2.7-Vp-p Driver IC Based on Functional Distributed Circuits for Optical Transmission Systems**

Y. Suzuki, Z.Yamazaki, H. Hida, System Devices Research Laboratories, NEC Corporation

A driver IC based on InP HBTs with new circuit topology – called functional distributed circuit (FDC) – for over 40-Gb/s optical transmission systems has been developed. The FDC topology enables both wider bandwidth and digital functions. The distributed differential amplifier stage in the developed driver IC exhibits 2.4-Vp-p (differential output: 4.8 Vp-p) output voltage swings and good eye openings at 50 Gb/s. Integrated with a 2:1 selector, the driver IC produces 2.7-Vp-p (differential output: 5.4 Vp-p) output-voltage swings with high signal quality at 80 Gb/s. This is equivalent to the highest data rate operation yet reported. These results indicate that the FDC has the potential to realize high-speed and functional ICs for over-40-Gb/s transmission systems.

Monday June 13, 2005
3:30 PM
LBCC – Room103A/103B
Session RM04D: UWB

Chair: Srenik Mehta, Atheros Communications
Co-Chair: David Lovelace, PropheSi Technologies Inc.

RM04D-1 3:30 PM Invited
Design Challenges in Emerging Broadband Wireless Systems

R. Gharpurey, Department of Electrical Engineering and Computer Science, University of Michigan

Broadband wireless systems are recent additions to the commercial application space. These systems are characterized by channel bandwidths that are a significant fraction of the carrier frequencies employed. An example of such a system is Ultra Wideband that uses a spectrum from 3.1-10.6GHz. Such systems introduce new circuit design challenges because of the potential requirement for simultaneously achieving high bandwidth and dynamic range.

RM04D-2 3:50 PM
A 5.4-mW LNA Using 0.35-um SiGe BiCMOS Technology for 3.1-10.6-GHz UWB Wireless Receivers

Ming-Da Tsai, Kun-You Lin, and Huei Wang, National Taiwan University

A modified low-power and low-noise distributed amplifier for ultra-wideband (UWB) radio systems is first proposed to overcome the bottleneck of conventional DA. The UWB LNA achieves 10-dB and 12-dB gain with 5.4-mW and 9-mW power consumption, respectively, and 3-dB roll off up to 10.6 GHz. The measured noise figures are lower than 5.5 dB from 3.1 to 10.6 GHz with 1.5 V supply. The MMIC occupies total chip size of only 0.47 mm² including all testing pads.

RM04D-3 4:10 PM
A 0.25-mm CMOS Ultra-Wideband Amplifier for Time-Domain UWB Applications

X.Guan,C.Nguyen, Texas A&M University

An ultra-wideband (UWB) amplifier has been developed using a standard low cost 0.25-mm CMOS process for UWB applications. Finite-ground coplanar waveguide (CPW) is used for easy shunt connection and low loss. The developed UWB amplifier works over the entire ultra-wide bandwidth of 3.1-10.6 GHz under non-sinusoidal time-domain signal operation needed for UWB systems. The amplifier was designed and characterized completely in the time domain. Time-domain measurement results show gain around 6 dB and return loss greater than 13 dB. The UWB CPW CMOS amplifier has linear phase and produces amplified signals, which resemble faithfully the input UWB non-sinusoidal pulses, demonstrating its suitability for time-domain UWB applications.

RM04D-4 4:30 PM**A 3.1-10.6 GHz RF Front-End for MultiBand UWB Wireless Receivers**

B. Shi and Michael, Y. W. Chia, Institute for Infocomm Research

This paper describes the design of a 3.1-10.6 GHz RF front-end for multiband UWB wireless receivers. The designed front-end chip was fabricated in a 0.25 μ m SiGe BiCMOS technology and assembled in a low-cost 24-lead LPCC package. Powered by a 2.7 V supply with 31 mA current consumption, the front-end delivered 20.6-21.8 dB of power gain and 4.1-6.2 dB of double-sideband noise figure over the entire 3.1-10.6 GHz UWB frequency band, respectively, and achieved an input IP₃ of -12.7 dBm at 3.3GHz.

RM04D-5 4:50 PM**A Low Power Noncoherent CMOS UWB Transceiver ICs**

Yuanjin Zheng*, Yan Tong*,**, Jiangnan Yan*,**, Yong-Ping Xu**, Wooi Gan Yeoh*, Fujiang Lin*, *Institute of Microelectronics, Singapore Science Park II, 117685, Singapore, **National University of Singapore, 117576, Singapore

A fully integrated pulse based UWB transmitter and receiver (TRX) using a novel and simple noncoherent architecture is presented. Fabricated in a 0.18- μ m CMOS process, the signal from the transmitter is binary amplitude modulated pulses and meets FCC UWB low frequency band (3.1-5GHz) specification. The receiver archives a noise figure of 7.5dB, IIP₃ of -14dBm, and sensitivity of -72dBm. The TRX can attain a transmission rate up to 50Mbps and consumes 41.4mW average power.

Tuesday June 14, 2005

8:00 AM

LBCC – Room101

Session RTU1A: Low Power Wireless Data Systems

Chair: Stephen Lloyd, Beceem Communications, Inc.

Co-Chair: Glenn Chang, MaxLinear

RTU1A-1

8:00 AM

Invited

Challenges in the Design of CMOS Transceivers for the IEEE 802.11 Wireless LANs: Past, Present and Future

Masoud Zargari, Srenik Mehta, David Su, Atheros Communications

This paper presents the challenges involved in the design of integrated IEEE 802.11 wireless LAN transceivers with focus on radio architecture and circuit implementation. In particular, examples of critical blocks in receiver and transmitter will be discussed.

RTU1A-2

8:20 AM

Invited

Low Power RF Design for Sensor Networks

Ben W. Cook, Alyosha Molnar, Kristofer S. J. Pister, University of California-Berkeley

Design of RF circuits for short-range, low data-rate wireless communication is discussed. A derivation of optimum design parameters is presented based on simple models for indoor path loss and power vs. performance tradeoffs in a generic transceiver. Design techniques aimed at efficiently reaching these parameters are discussed for individual circuit blocks. Finally, a review of some proposed transceiver implementations is reported.

RTU1A-3 8:40 AM**A Long-Range RFID IC with On-chip ADC in 0.25 μ m CMOS**

F. Kocer, M. P. Flynn, Wireless Integrated Microsystems Engineering Research Center (WIMS-ERC) , University of Michigan, Ann Arbor

This 1mm² wireless telemetry device recovers power and a reference clock from a 450 MHz incident RF signal and returns data as a binary phase shift keyed signal on a 900 MHz carrier. The device generates a 3 VDC supply from a -12.3 dBm incident RF signal. This corresponds to an operating distance of more than 18 meters in the US. The transmit data includes the output of an on-chip 5-bit single-slope analog-to-digital converter (ADC) and a 3-bit ID tag. The entire IC dissipates 4mW while active.

RTU1A-4 9:00 AM**A CMOS 2.45-GHz Radio Frequency Identification Tag IC with Read/Write Memory**

W.G. Yeoh, Y.B. Choi, K.Y. Tham, S.X. Diao*, Y.S. Li*, Institute of Microelectronics, Singapore * Toppan Electronics Co., (S) Pte. Ltd., Singapore

A 2.45-GHz RFID tag chip was designed on standard 0.25- μ m CMOS process. Using only MOS devices, the low-V_t rectifier circuit produces 100 μ W of power with 2dBm input. The tag IC with bi-directional communication and anti-collision features can be read from a distance of up to 15cm under a reader power of 250mW. The die area of 0.79mm² includes a 128-bit rewriteable non-volatile memory.

RTU1A-5 9:20 AM Invited**A Fully Integrated SOC for 802.11b in 0.18 μ m CMOS**

H. Darabi, S. Khorram, Z. Zhou, T. Li, B. Marholev, J. Chiu, J. Castaneda, E. Chien, S. Anand, S. Wu, M. Pan, R. Rofougaran, H. Kim, P. Lettieri, B. Ibrahim, J. Rael, L. Tran, E. Geronaga, H. Yeh, T. Frost, J. Trachewsky, A. Rofougaran, Broadcom Corp.

A fully integrated system-on-a-chip intended for use in 802.11b applications is built in 0.18 μ m CMOS. All the radio building blocks including PA, PLL loop filter, and the TR switch, as well as the complete physical layer and the MAC sections have been integrated into a single chip. The radio tuned to 2.4GHz dissipates 165mW in receive-mode and 360mW in transmit-mode. The receiver achieves a sensitivity of \approx 88dBm at 11Mbps rate, and the transmitter delivers a nominal output power of 13dBm.

Tuesday June 14, 2005

8:00 AM

LBCC – Room102A/102B

Session RTU1B: Advanced RFIC Device Technology

Chair: Eli Reese, TriQuint Semiconductor

Co-Chair: Mahesh Kumar, Lockheed Martin

RTU1B-1 8:00 AM

High Power Density InGaP PHEMTs for 26 V Operation

E. Lan, B. M. Green, P. Li, O. Hartin, P. Fisher, D. Maurer, P. M. Piel*,
B. Knappenberger, M. Cde. Baca, M. Miller*, and C. E. Weitzel, Freescale
Semiconductor, Inc., Microwave and Mixed Signal Technologies
Laboratory, *RF Division

This paper presents a high power density and high efficiency InGaP barrier PHEMT technology for 26 V operation. This device was evaluated for 3G infrastructure applications at 2.14 GHz and WiMAX applications at 3.5 GHz. Power density, efficiency, and IM₃ are superior to that of the InGaP channel FETs reported before.

RTU1B-2 8:20 AM

RF MEMS: status of the industry and roadmaps

Jeremie Bouchaud, Henning Wicht, WTC-Wicht Technologie Consulting

RF MEMS have entered the commercialization phase in 2003. BAW filters are already produced in series and first commercial switches are available. Though, reliability and packaging problems are still a major hurdle. The presentation will give an overview on RF MEMS applications and market players and highlight technical challenges that still have to be solved to open mass markets such as mobile telephony and WLAN. WTC will also present applications of RF MEMS and opportunities in niche markets.

RTU1B-3 8:40 AM**A Novel RF High-Q Metal-Semiconductor-Metal Planar Inter-Digitated Varactor Based on Double-Channel AlGaIn/GaN HEMT Structure**

C. S. Chu, Y. G. Zhou, K. J. Chen, K. M. Lau, Hong Kong University of Science and Technology

A novel GaN-based Double-Channel Metal-Semiconductor-Metal Configuration Planar Inter-Digitated varactor fabricated with HEMT compatible process is presented. Our varactors achieved high Q-factor, wide tuning range and high minimum Q-factor (Q_{min}). The double-channel heterostructure extends the useful high Q-factor capacitance tuning range of the varactors. The measurement results of the novel double-channel varactors are compared with the varactors fabricated on single channel heterostructure.

RTU1B-4 9:00 AM**Low-Distortion, Low-Loss Varactor-Based Adaptive Matching Networks, Implemented in a Silicon-on-Glass Technology**

K. Buisman, L.C.N. de Vreede, L.E. Larson*, M. Spirito, A. Akhnouk, Y. Lin, X. Liu, L.K. Nanver, DIMES, Delft University of Technology, Delft, The Netherlands, *University of California, San Diego, Center for Wireless Communications

A low-loss, low-distortion continuously tunable matching network, is demonstrated at 2 GHz in a silicon-on-glass varactor IC technology. The tuner uses an optimized varactor configuration to minimize distortion, and exhibits less than 0.5 dB loss and $IM_3 < -50$ dBc at 27 dBm output power, and tunes with a VSWR $> 250:1$ to 1:1.

Tuesday June 14, 2005
8:00 AM
LBCC – Room102C
Session RTU1C: CMOS VCOs

Chair: Stephen Dow, ON Semiconductor
Co-Chair: Dan Nobbe, Peregrine Semiconductor

RTU1C-1 8:00 AM Invited
Designing an Ultra Low Phase Noise 4.5 GHz VCO
Using Multiple Coupled Resonators and MOS Devices
U.L. Rohde, Synergy Microwave Corp., Inc.

This paper shows a 4.5 GHz center frequency push-pull oscillator based on the use of NMOS and PMOS transistors, the use of multiple-coupled resonators as tuned elements, and source RF feedback for improved phase noise. Two MOS transistors are used as varactors. At 5 GHz and 1 MHz offset, the phase noise is ~ 118 dBc/Hz. This paper gives detailed insight in to the design procedure of the oscillator including the device selection.

RTU1C-2 8:20 AM
RF CMOS Differential Oscillator with Source
Damping Resistors

Choong-Yul Cha, Hyoung-Chul Choi, Hoon-Tae Kim and Sang-Gug Lee,
Samsung Advanced Institute of Technology, *Samsung Electronics,
**Information and Communications University

This paper proposes a new method to suppress $1/f$ noise contribution of active devices in oscillator using source damping resistors. The operational mechanism of proposed source damping resistor method is analyzed through circuit simulation with complementary LC differential oscillator topology. This analysis shows that the amount of $1/f$ noise and the mismatch of instant current swing of oscillator's active devices can be substantially reduced with source damping resistors. The reduced $1/f$ noise???

RTU1C-3 8:40 AM**Phase Noise Optimization of CMOS VCO through Harmonic Tuning**

Seonghan Ryu, Yujin Chung*, Huijung Kim, Jinsung Choi and Bumman Kim, Pohang University of Science and Technology, *Samsung Electronics

An optimization technique for a low phase noise CMOS LC VCO is proposed. The combination of harmonic tuning and on-chip filtering improves both $1/f^3$ and $1/f^2$ phase noise more than 10dB over a comparable reference VCO. A 2.7V, 5.4mA, 30% tuning range, 1GHz VCO is designed with the technique and implemented in a 0.35 μ m CMOS process. The optimized 1GHz CMOS differential VCO achieves -89dBc/Hz, -116dBc/Hz and -135dBc/Hz at 10KHz, 100KHz, and 1MHz offset frequencies from the carrier, respectively.

RTU1C-4 9:00 AM**Noise Contributors in a Low Power VCO with Automatic Amplitude Control**

R. Murji and J. M. Deen, McMaster University

In this paper the major noise sources in a VCO with automatic amplitude control (AAC) circuit, fabricated in a commercial CMOS deep n-well 0.18 μ m technology allowing access to the body of NMOS transistors is described. The analysis shows that there is an optimal point where the noise due to the AAC is minimal and thus equivalent to a VCO with no AAC. The oscillator consumes 4.32 mW@1.8 V, has a tuning range of 410 MHz and a phase noise level of -108 dBc/Hz@1 MHz from a 7.2 GHz carrier.

RTU1C-5 9:20 AM**A 9.953/10.7/12.5GHz 0.13 μ m CMOS LC Oscillator Using Capacitor Calibration and a VGS/R Based Low Noise Regulator**

A. Maxim, D. Lazlo, Integrated Products, Fiber Communications Division, Austin, TX

A 0.13 μ m CMOS low phase noise multi-rate LC oscillator for 10Gbps communications. To minimize the gain, the frequency is first calibrated to within $\pm 0.1\%$ of the target value and then the final locking is achieved with MOS varactors having a $\pm 1\%$ tuning range. A high PSRR and low noise VGS/R based regulator was used to bias the oscillator. The LC-VCO specifications include: phase noise < -115 dBc/Hz at 100KHz offset, $1/f^3$ corner frequency < 40 KHz, current < 10 mA from a 3.3V supply and 250x400 die area.

Tuesday June 14, 2005

8:00 AM

LBCC – Room103A/103B

Session RTU1D: Switching Class Power Amplifiers

Chair: Freek van Straten, Philips Semiconductors

Co-Chair: Bruce Thompson, Motorola Labs

RTU1D-1 8:00 AM Invited

Next Generation Power Amplifiers for Wireless Communications - Squeezing More Bits from Fewer Joules

L. E. Larson, P.A. Asbeck, D. Kimball, University of California, San Diego

This paper covers the limitations of current handset power amplifier design. The specific limitations on efficiency and linearity are addressed, and several of the most promising techniques for improvements are discussed.

RTU1D-2 8:20 AM

GaAs HBT Class-E Amplifiers for 2-GHz Mobile Applications

E. A. Jarvinen, M. J. Alanen, Nokia Technology Platforms

This paper discusses practical design aspects of integrated class E power amplifiers. The described design concepts were applied to the realization of a two-stage GaAs HBT amplifier targeted for WCDMA operation. The fabricated MMIC was packaged in a 12-load ad 3x3 mm² MLF package, which was mounted onto a FR4 test board. At the center frequency of 1.95 GHz the power amplifier delivered an output power of 27.0 dBm with a collector and power-added efficiencies of 74.5% and 62.5%, respectively.

RTU1D-3 8:40 AM**A 1.4 GHz - 2 GHz Wideband CMOS class-E Power Amplifier Delivering 23 dBm Peak With 67% PAE**

A. Mazzanti, L. Larcher*, R. Brama*, and F. Svelto**, DII University of Modena and Reggio Emilia, *DISMI University of Modena and Reggio Emilia, **DIE University of Pavia

Efficiency is one of the key requirements in PA designs, but it is usually obtained at the expense of large device stress. The cascode class-E PA, proposed in this paper, allows simultaneously high efficiency and reduced stress by means of an integrated inductor tuning out the typical parasitics of the cascode topology. Prototypes, realized in a 0.13 μm CMOS technology demonstrate 67% PAE while delivering 23 dBm peak power at 1.7 GHz. PAE is still above 60% within the range 1.4 GHz - 2 GHz.

RTU1D-4 9:00 AM**Class E Amplifier with Inductive Clamp Circuit**

A. Eroglu, D. Lincoln, MKS ENI Products

A Class E RF amplifier which can operate into any load conditions without need for other additional circuitry to protect transistors is introduced. This is provided by the new topology which incorporates inductive clamp circuitry to the basic Class E amplifier circuit. Class E amplifiers with this topology can be used in plasma applications where the load conditions are dynamic.

RTU1D-5 9:20 AM**An Adaptive Protection Circuit for Power Amplifier Ruggedness Improvement**

W. Karoui*,**, P. Riondet*, T. Parra**, G. Montoriol*, *Freescale Semiconductors, **LAAS-CNRS

This paper presents a monolithically integrated, cost and size effective protection circuit based on collector current limitation for GaAs HBT PA ruggedness improvement. Compared with other conventional protection circuits such as voltage limiters, the proposed circuit does not involve complex circuits which are expensive and take a valuable space. The experimental results show that the PA ruggedness was improved while maintaining the output power and power-added efficiency on a 50 Ohms load.

Tuesday June 14, 2005

1:20 PM

LBCC – Room101

Session RTU3A: RF High Power Circuit Blocks

Chair: David Ngo, RF Micro Devices, Inc

Co-Chair: Noriharu Suematsu, Mitsubishi Electric Corp.

RTU3A-1

1:20 PM

Invited

Fully Integrated CMOS RF Power Amplifiers - A Prelude to Full Radio Integration

Ali Hajimiri, California Institute of Technology, Pasadena, CA, USA

A fully integrated radio on a chip offers innumerable advantages and several challenges. In this article, we will discuss some of these opportunities and challenges for a fully-integrated CMOS PA and see how the distributed active transformer (DAT) technology can overcome them.

RTU3A-2

1:40 PM

Differential CMOS Linear Power Amplifier with 2nd Harmonic Termination at Common Source Node

Jongchan Kang, Yisun Chung*, Sungbo Hwang* and Bumman Kim, Pohang University of Science and Technology in Korea, , *MagnaChip Semiconductor Ltd. in Korea

In this paper, we present a 2.45GHz fully-differential CMOS power amplifier (PA) with high efficiency and linearity. We have adopted a 0.18 μ m standard CMOS process with Cu-metal and all components of the 2-stage circuit are integrated into one chip. To improve the linearity, we newly adopt the harmonic termination technique at the common source along with normal harmonic termination at the drain. The harmonic termination at the source suppresses the second harmonic generated at the input Cgs. The amplifier shows 17.5dB of power gain and 20.5dBm of P1dB with 37% of PAE. Linearity measurements from 2-tone test show that the power amplifier with the second harmonic termination at the source improves maximum 6dB of IMD3 and 7dB of IMD5 over the amplifier with harmonic termination at the drain only. Furthermore, the linearity improvements appear over entire range of the power level and the linearity maintains low below -45dBc of IMD3 and -57dBc of IMD5 for an output power backed-off more than 5dB from P1dB.

RTU3A-3 2:00 PM**On the Optimum 2nd Harmonic Source and Load Impedances for the Efficiency-linearity Trade-off of LDMOS Power Amplifiers**

D.M.H. Hartskeerl*, I. Volokhine*, and M. Spirito**, * Philips Research Laboratories, ** HiTEC Laboratory, Delft University of Technology

For the first time a systematic analysis on the simultaneous impact of the second harmonic source and load terminations on the linearity-efficiency trade-off of LDMOS power amplifiers (PAs) is presented. For the combinations studied it can be concluded that, contrary to common design practice, open-circuiting both the in- and output of a RF LDMOS PA at the second harmonic frequency results in the best trade-off. On-wafer large-signal measurements with the above-mentioned optimal impedances have

RTU3A-4 2:20 PM**A Miniature Low-Insertion-Loss, High-Power CMOS SPDT Switch Using Floating-Body Technique for 2.4- and 5.8-GHz Applications**

Mei-Chao Yeh, Ren-Chieh Liu, Zuo-Min Tsai and Huei Wang, National Taiwan University

A low insertion loss SPDT switch using body-floating technique in standard 0.18- μm CMOS process was developed for 2.4- and 5.8-GHz WLAN applications. The switch achieves a measured P1dB of 20 dBm, an insertion loss of 1.1 dB, and an isolation of 27 dB at 5.8 GHz. It also achieves a measured insertion loss of 0.65 dB and an isolation of 35 dB at 2.4 GHz. The effective chip size is 0.03 mm².

RTU3A-5 2:40 PM**An Ultra-Low Distortion 3P2T Antenna Switch MMIC for Dual-band W-CDMA Applications**

E.Yasuda,K.Hidaka,T.Nakatsuka,A.Watanabe,K.Tara, RF-Semiconductor Development Center, Matsushita Electric Industrial Co., Ltd.

An ultra-low distortion 3P2T antenna switch MMIC for dual-band W-CDMA systems has been developed. Ultra-low distortion and low insertion loss were achieved by controlling 2-stacked FETs with 7V which is up-converted from a supply voltage of 2.4V using Si charge pump circuit. The switch MMIC provides IMD2 and IMD3 levels less than -110dBm, which well satisfies the out-of-band blocking specification for W-CDMA systems. The insertion losses are 0.27dB for 800MHz and 0.38dB for 2GHz.

Tuesday June 14, 2005
1:20 PM
LBCC – Room102A/102B
Session RTU3B: Frequency Generation Circuits II:
New Concepts and
Building Blocks

Chair: Sanjay Raman, Virginia Tech
Co-Chair: Huei Wang, National Taiwan University

RTU3B-1 1:20 PM

A 40GHz 2.1V Static Frequency Divider in SiGe Using a Low-Voltage Latch Topology

D. Kucharski, K. T. Kornegay, Cornell University

An alternative low-voltage latch topology based on switched emitter followers is proposed and its characteristics are compared to a traditional current-mode latch. A static 1:8 frequency divider is implemented in a 120GHz SiGe BiCMOS technology using the proposed latch. The divider operates at the maximum frequency of 42GHz and consumes 160mW from a 2.1V power supply.

RTU3B-2 1:40 PM

A Low-Power 17-GHz 256/257 Dual-Modulus Prescaler Fabricated in a 130-nm CMOS Process

Yanping Ding, Department of Electrical and Computer Engineering, University of Florida

A divide-by 256/257 dual-modulus prescaler has been fabricated in a 130-nm CMOS process. The synchronous divide-by-4/5 divider uses source coupled logic (SCL) D flip-flops with a resistive load to achieve the 17.2- GHz maximum operating frequency at input power of 0dBm, The prescaler requires 4.3 mA current from a 1.5-V supply. This circuit has the highest operating frequency and the lowest power consumption reported to date among CMOS dual-modulus prescalers that can operate at 10 GHz or higher. The prescaler also works up to 15.8 GHz with a 1.2-V supply and draws 3-mA current.

RTU3B-3 2:00 PM**Variable Division Ratio of a 20 GHz CMOS Injection-Locked Frequency Divider**

F. H. Huang, D. M. Lin, H. P. Wang, W. Y. Chiu and Y. J. Chan, Department of Electrical Engineering, National Central University, Taiwan R.O.C.

A variable division ratio injection-locked frequency divider (ILFD), controlled by the input offset voltage, was realized using the 0.13 μ m CMOS technologies. In this report the controllable division ratios were made from 2 up to 16 with an input ac signal of 10 GHz, by changing the input dc offset voltages. This divider also performs the division ratios of 2, 4, 6 and 8 wide locking range up to 20 GHz at a 2.5 GHz self-oscillation. The dc supplied voltage of circuit is only 2V and the dividing capability can reach 20 GHz.

RTU3B-4 2:20 PM**Time-to-Digital Converter for RF Frequency Synthesis in 90 nm CMOS**

R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. T. Balsara*, Wireless Analog Technology Center, Texas Instruments Inc., *Center for Integrated Circuits and Systems, Univ. of Texas at Dallas

We present a 20 ps time-to-digital converter (TDC) in 90 nm digital CMOS. It is used as a phase/frequency detector and charge pump replacement in an all-digital PLL for a single-chip fully-compliant GSM transceiver. The TDC consumes 1.3 mA at 1.3 V. Measured INL is 0.7 LSB.

RTU3B-5 2:40 PM**Toward Wireless Receivers Without Crystals**

F. L. Martin, P. Gorday, D. Taubenheim, Motorola Labs

Emerging technologies which can be applied to the crystalless receiver problem are reviewed. A receiver architecture, based on differential chip detect of a direct-sequence spread spectrum, is described. A novel, fully-integrated crystalless synthesizer architecture is presented. The combination of the synthesizer and receiver mitigate synthesizer noise and frequency offset using a code length of at least 32 chips.

Tuesday June 14, 2005

1:20 PM

LBCC – Room102C

Session RTU3C: RF Trends

Chair: Stefan Heinen, RWTH Aachen University

Co-Chair: Luciano Boglione, Filtronic Sigtek

RTU3C-1

1:20 PM

Invited

Multi-Mode, Multi-Band RF Transceiver Circuits for Mobile Terminals in Deep-submicron CMOS Processes

Bertan Bakkaloglu, Paul A. Fontaine, Texas Instruments Inc.

Circuit design techniques, architectures and characterization results for RF and analog circuits for multi-mode, multi-band (GSM900/DCS1800/PCS1900/UMTS) single-chip RF transceivers are presented. Reported circuits are designed in 90nm standard digital COS process with no additional analog components. Critical RF and analog design parameters are derived for direct conversion multi-mode transceivers based on UMTS and GSM/DCS/PCS standards. Discrete component specifications are derived based on I???

RTU3C-2

1:40 PM

A Direct Up-Conversion Transmitter with Integrated Prescaler for Reconfigurable Multi-Band/Multi-Standard

J. Platz*, G. Strasser*, K. Feilkas**, L. Maurer***, A. Springer*#, *LCM Linz Center of Mechatronics GmbH, **Infineon Technologies AG, ***DICE Danube Integrated Circuits Engineering, #Inst. for Communications and Information Engineering University of Linz

A direct up-conversion transmitter IC for reconfigurable multi-band/multi-standard base stations is presented. The chip consists of a quadrature modulator, an baseband filter, and a reconfigurable prescaler which provides three divider-ratios. The up-converter was designed for a frequency range of 400MHz to 2.7GHz.

Measurements show an maximum output channel power of -1.9dBm and an ACLR lower -57dBc. The measured EVM is lower than 2.2% and the noise floor has an upper limit of -153dBm/Hz.

RTU3C-3 2:00 PM**Multiband Multi-Standard Transmitter using a Compact Power Amplifier Driver**

H. Magnusson, H. Olsson, Royal Institute of Technology (KTH), Stockholm, Sweden

This paper presents a multistandard transmitter solution using a new power amplifier (PA) [1] driver operating in the broadcast, mobile, and the 2&5 GHz ISM bands. The use of dual-loop feedback in the driver provides a matched output without area consuming matching networks. The circuit size is as small as 0.3 mm², saving about 0.7 mm² silicon area. Measurement results show a gain higher than 7.8 dB with a maximum output power of +4 dBm for all bands and using a supply voltage of 1.8V.

RTU3C-4 2:20 PM**Temperature Effect on the Performance of a Traveling Wave Amplifier in 130 nm SOI Technology**

M. Si Moussa* Member, IEEE, C. Pavageau**,***, F. Danneville** Member, IEEE, J. Russat***, N. Fel***, J.-P. Raskin* Member, IEEE and D. Vanhoenacker-Janvier* Senior Member, IEEE, * EMIC ñ UCL BELGIUM, ** IEMN ñ FRANCE, *** CEA - FRANCE

The behavior of an integrated traveling wave amplifier(TWA) fabricated on 130nm Silicon-on-Insulator(SOI)CMOS process has been characterized over a temperature range from 25 C to 250 C. The TWA is a four-stage cascode design which uses Floating Body (FB) transistors and microstrip lines as passives. A gain of 7dB with a 0.4-27GHz bandwidth is measured under 1.4V supply voltage. The effects of high temperature are observed on the gain of the TWA, as well as on the SOI transistors and the TFMS lines.

Tuesday June 14, 2005

1:20 PM

LBCC – Room103A/103B

Session RTU3D: Receiver Circuits

Chair: Reynold Kagiwada, Northrop Grumman

Co-Chair: Tadao Nakagawa, NTT

RTU3D-1

1:20 PM

Invited

Low Voltage Techniques for sub 100nm CMOS, RF Transceivers

K. Soumyanath, Intel Corp.

Sub 100nm CMOS provides high f_T and f_{max} devices that offer many advantages for RFIC design. However, these benefits come with the necessity of using low supply voltages ($\sim 1.2V$) and low resistivity substrates. In this paper, we describe circuit techniques for WLAN components (LNAs, synthesizers, filters and ADC front ends) that overcome these constraints while fully realizing the advantages of scaled CMOS

RTU3D-2

1:40 PM

A 2GHz-Band Self Frequency Dividing Quadrature Mixer

E. Taniguchi, C. Kageyama, N. Suematsu, Information Technology R&D Center, Mitsubishi Electric Corporation

A 2GHz-band self frequency dividing quadrature mixer(SFDQM) is proposed. The SFDQM uses a static-type 1/2 frequency divider as LO switching circuit, and needs no external 90 degree phase shifter. Since this mixer can eliminate a 90 degree phase shifter and one of the unit mixer blocks having a LO amplifier, it realizes very low power consumption and very small die area on IC chip. The SFDQM is fabricated in 0.35 μm SiGe-BiCMOS technology and its down conversion characteristics are evaluated.

RTU3D-3 2:00 PM**An Antenna Switch MMIC for GSM/UMTS Handsets Using E/D-Mode JPHEMT Technology**

K. Kohama, M. Nakamura, K. Onodera, S. Wada, S. Tamari, Y. Mizunuma, Sony Corporation Semiconductor Solutions Network Company

An antenna switch MMIC, having SP7T configuration, for quad band GSM/UMTS handsets using enhancement mode and depletion mode junction gate pHEMT (E/D-mode JPHEMT) technology has been developed. The high gate turn-on voltage enables a novel ESD protection device (P-EFET) and a logic circuit to integrate with an antenna switch without degradation in the RF performance. Sufficiently high ESD robustness is achieved as well as excellent RF performance.

RTU3D-4 2:20 PM**Resistive Mixers for Reconfigurable Wireless Front-ends**

R. Circa, D. Pienkowski, G. Boeck, R. Kakerow*, M. Mueller*, R. Wittmann*, Technische Universitat Berlin, Microwave Engineering Group, Einsteinufer 25, 10587 Berlin, Germany, *Nokia Research Center, Bochum, Germany

Two resistive mixers realized in a 0.13 μm HCMOS process will be presented in this paper. The mixers are designed for implementation in a reconfigurable mobile terminal that supports the WCDMA mobile phone standard and the IEEE802.11a and HIPERLAN/2 WLAN standards, respectively. The mixer design process as well as simulated and measured results are given and discussed. The entirety of properties and performance make these mixer types very attractive for reconfigurable architectures

RTU3D-5 2:40 PM**A 45-degree CMOS Phase Shifter and Gain/Phase Imbalance Compensation for Multi-Band Transceivers**

T. Nakagawa, M. Kawashima, M. Matsui, K. Araki, NTT Network Innovation Laboratories, NTT Corporation

This paper presents two approaches to achieve multi-band modulators and demodulators for direct conversion architecture. One is a 45-degree CMOS phase-shifter, whose input frequency is $4/3$ times the desired frequency. The proposed circuit diagram makes impossible to have a lower input frequency than conventional 45-degree phase shifters that use frequency dividers. The other is a gain/phase compensation method. Compensation procedures involving an actual demodulator were successfully performed.

Tuesday June 14, 2005

3:30 PM

LBCC – Room101

Session RTU4A: Silicon Integrated VCOs

Chair: Ting-Ping Liu, Winbond Electronics (Shanghai)

Co-Chair: Yann Deval, IXL lab

RTU4A-1 3:30 PM

The Effect of Substrate Noise on VCO Performance

N. Checka, D. Wentzloff, A. Chandrakasan, R. Reif, Microsystems
Technology Laboratories, MIT

The effect of substrate noise on the performance of voltage controlled oscillators (VCO) as a function of circuit isolation, bias current, and center frequency is presented. Guard rings provide as much as 25 dB of isolation for the 900 MHz VCO down to 1dB of isolation for the 5.2 GHz VCO.

RTU4A-2 3:50 PM

Design and Optimization of a Linear Wide-band VCO for Multimode Applications

A. Koukab, Y. Lei, M. Declercq, Ecole Polytechnique Fédérale de Lausanne (EPFL) Laboratoire d'Électronique Générale (LEG-IMM).contact: adil.koukab@epfl.ch

An LC VCO designed in 0.25 μ m BiCMOS-SiGe process achieves a tuning range 2.8GHz-3.75GHz while drawing 1.3 mA from 2.5V supply. Two self-calibrations methods are proposed, analyzed and their circuits are integrated to compare their measured performances. This comparative study shows that for the same low VCO gain, the number switched-capacitor units can be reduced from 15 (4 bits) in the conventional calibration approach to 1 in the proposed linearization based approach.

RTU4A-3 4:10 PM**I/Q LC Oscillators with an Octave Tuning Range for TV on Mobile Platforms**

Johan van der Tang, Roger Amiot*, Harm Rump* Dieter Kasperkovitz*, Arthur van Roermund, Eindhoven University of Technology, Semiconductor Ideas to the Market (ItoM)*

Two novel I/Q oscillators have been realized that cover one octave tuning range, and when combined with a divider and a multiplexer, cover the complete TV band. The realized oscillators embody highly cost-effective key building blocks for tuning systems in consumer ICs for TV on portable platforms.

RTU4A-4 4:30 PM**Design of Quadrature CMOS VCO using Source Degeneration Resistor**

Seong-Mo Moon, Moon-Que Lee, Byung-Sung Kim*, University of Seoul, 90 Cheonnong-dong, Dongdaemun-gu, Seoul, 130-743, Korea, *Sungkyunkwan University, Suwon, Korea

A new schematic of QVCO is designed and fabricated. To obtain quadrature characteristic and low phase noise simultaneously, two differential VCOs are forced to run in quadrature mode by using cross-coupled transistor with a source degeneration resistor, which is optimized to obtain quadrature accuracy with minimum phase noise. The measured performance showed the phase noise of below ≤ 120 dBc/Hz at 1 MHz frequency offset, tuning bandwidth of 210 MHz with a tuning voltage varying from 0 to 1.8 V.

RTU4A-5 4:50 PM**A Low-Phase-Noise Wide-Band CMOS Quadrature VCO for Multi-standard RF Front-Ends**

Ali Fard and Pietro Andreani*, Mälardalen University, Dept. of Electronics, Västerås Sweden, *Technical University of Denmark, Center for Physical Electronics, Ørsted-DTU, Denmark

A low phase noise LC QVCO with a wide frequency range of 3.6-5.6GHz for multi-standard front-ends is presented. A significant advantage of the topology is the larger oscillation amplitude when compared to other conventional QVCO structures. The QVCO is compared to a double cross-coupled LC-tank differential oscillator both in theory and experiments for evaluation of its phase noise. Measurements show a phase noise level of -127.5 dBc/Hz at 3MHz offset from a 5.6GHz carrier while dissipating 8 mA.

Tuesday June 14, 2005
1:30 PM
LBCC – Grand Ballroom
Session RTUIFR: Interactive Forum

Chair: Freek van Straten, Philips Semiconductor
Co-Chair: Andre Hanke, Infineon Technologies

RTUIFR-01

A 3 – 10 GHz SiGe Resistive Feedback Low Noise Amplifier for UWB Applications

Jongsoo Lee and John D. Cressler, School of Electrical and Computer Engineering, 777 Atlantic Drive, N.W., Georgia Institute of Technology, Atlanta, GA, 30332-0250, USA

The analysis and design of an inductorless, resistive feedback low noise amplifier using advanced SiGe HBT technology, for application in UWB systems is presented. Measurements show 20dB of gain with 1dB variation over the 3GHz to 10GHz band, and a matched input and output with less than -10dB of reflection. A minimum noise figure is 3.05dB at 3GHz and increases to 4.5dB at 10GHz with 3x smaller die size compared to conventional LNA. Measured IIP₃ is -11.75dBm at 17mA from 2.5V supply.

RTUIFR-02

Consideration of Age Degradation in the RF Performance of CMOS Radio Chips for High Volume Manufacturing

M. Ruberto, T. Maimon, Y. Shemesh, A. Baguenier Desormeaux*, W. Zhang**, and C. Yeh**, Wireless Products Division, Intel Corporation, *Cadence Design Systems SAS, **Cadence Design Systems, Inc.

Age reliability in the RF performance of CMOS radio chips must be validated prior to high volume manufacturing. We show the results of age simulations on some RF subblocks used in our 802.11a/b/g radio chip for our WLAN card. RF aging effects on a driver amplifier and a mixer design were simulated using Cadence's RelXpert, which allows for age modeling from the single transistor level up to the entire TX/RX chain hierarchies. The NMOS/PMOS models used accounted for HCI and NBTI age degradation.

RTUIFR-03

Modeling of Broadband Noise in Complementary (nnp + pnp) SiGe HBTs

B. Banerjee, S. Venkataraman, E. Zhao, C.-H. Lee, J. D. Cressler, J. Laskar, B. E.-Kareh*, S. Balster*, H. Yasuda*, Georgia Institute of Technology, *Texas Instruments

The first comprehensive investigation of broadband noise in a complementary SiGe HBT BiCMOS technology is presented. A base-transit time based noise model with its origins in linear noisy two-port theory is presented, which takes into account the fundamental base and collector shot noises in a bipolar transistor and their cross-correlation. This noise model is compared with the conventional SPICE noise model and the differences in the noise behavior of the npn and pnp SiGe HBTs is analyzed.

RTUIFR-04

Fully Integrated Fractional PLL for Bluetooth Application

M. Marletta, P. Aliberti, M. Pulvirenti, A. Cavallaro, S. Terryn, P. Filoramo, R. Iardino, V. Spalma, S. Cosentino, STMicroelectronics

A fully integrated Sigma-Delta Fractional-N frequency synthesizer for Bluetooth application is presented. The synthesizer, suitable to be used with a wide range of crystal oscillator, features a settling time of 70us, a phase noise of 80 dBc/Hz and 125 dBc/Hz at 100 KHz and 1 MHz offset respectively. The fractional spurs are -63dBc at 1 MHz offset. The synthesizer is part of a 0.13-um CMOS single-chip application for v1.2 Bluetooth, which has been fully qualified between -40C till +85C.

RTUIFR-05

On-Wafer Characterization De-embedding and Transmission Line Optimization on Silicon for Millimeter-wave Applications

S.K. Rockwell, B.A. Bosco, Motorola Labs, Motorola Labs

The design and implementation of transmission line based calibration standards suitable for de-embedding on-wafer active and passive elements for millimeter-wave applications on silicon BiCMOS backend process technology is investigated. Loss mechanisms, accuracy requirements, layout considerations, and impedance dependent characteristics of transmission line structures are discussed.

Application of popular on-wafer, in situ calibration de-embedding approaches is evaluated. Methods to improve backend process technology for millimeter-wave applications are suggested based upon transmission modeling using EM simulation tools. Modeled versus measured results are presented in support of conclusions.

RTUIFR-06

A Compact Low Noise Amplifier in SiGe:C BiCMOS Technology for 40GHz Wireless Communications

S. Pruvost* **, I. Telliez*, F. Danneville**, A. Chantre*, P. Chevalier*, G. Dambrine**, S. Lepilliet**, *STMicroelectronics Central R&D Crolles France, **IEMN UMR CNRS 8520 DHS Villeneuve d'Ascq France

This paper demonstrates the feasibility of a low area, low consumption Low Noise Amplifier for 40GHz wireless communications. Using a simple approach due to the microstrip line characteristics, the compactness is one of the key features and the circuit area is less than 0.3mm². A gain of 23dB with an associated noise figure of 3.7dB at 40GHz was achieved under less than 20mW DC-power consumption. Finally, LNA linearity reports an OIP1 of 10dBm which allows a 1GHz bandwidth dynamic range of 65dB.

RTUIFR-07

Integrated Differential 2 GHz 2.7V Low-Noise Active Bandpass Filters on Silicon

Z. Sassi*, S. Darfeuille*, B. Barelaud*, L. Billonnet*, B. Jarry*, H. Marie**, N. T. Luan Le**, P. Gamand**, *IRCOM, University of Limoges., **Innovation Centre RF, Philips Semiconductors.

Silicon Technology in CMOS and BiCMOS processes are nowadays showing very interesting intrinsic characteristics. Two 2-GHz 2.7V differential filter topologies are designed and analyzed in this paper. The first circuit is a filter based on an LC-Q enhance topology. The second circuit is a fourth-order bandpass filter developed and realized using four inductors electrically coupled with MOSFETs. Philips QUBIC4 Si BiCMOS technology is used.

RTUIFR-08

A Multi-phase 10 GHz VCO in CMOS/SOI for 40 Gbits/s SONET OC-768 Clock and Data Recovery Circuits

D. Axelrad, E. de Foucauld, M. Boasis, P. Martin, P. Vincent, M. Belleville and F. Gaffiot*, CEA-LETI, *LEOM/Ecole Centrale de Lyon

We present a CMOS/SOI Multi-phase VCO based on a ring amplifier with LC resonators. This circuit is a key block of a 40Gbit/s serial communication system. Operating at a speed one-fourth of the nominal data rate, this CMOS architecture complies with SONET OC-768 standard. The VCO exhibits a 25% frequency tuning range from 10.2GHz to 13GHz. The core power dissipation is 26mW under a -1.2V supply voltage. The measured phase noise is better than -105dBc/Hz, at 1MHz offset, over the tuning range.

RTUIFR-09

Highly Linear, Varactor-less, 24GHz IQ Oscillator

M.A. Sanduleanu, E.Stikvoort, Philips Research Eindhoven

This paper presents a varactor-less, quadrature oscillator with high linearity. It is based on two identical sections comprising a differential Colpitts part and a coupling part. Tuning of the common-mode current and/or differentially changing the tail currents of the coupling and Colpitts parts can achieve the variation of the oscillation frequency. The oscillation frequency can be changed from 23GHz to 24.4GHz (10%) for a variation in bias current from 1mA to 2.25mA. The linearity in the whole tuning range is better than $\pm 1.5\%$. The measured phase-noise @ 1MHz is about -94dBc/Hz . At a nominal supply voltage of $3.3\text{V} \pm 10\%$ the supply pushing is better than 250MHz/V . The IQ VCO has been realized in a BiCMOS process (QUBIC4) with 38GHz f_T and 3mm thick top metal layer for inductors. The occupied area is 0.23mm^2 and the power consumption is 22mW . Possible applications for this oscillator are IQ down-converters, transceivers for mm-Wave and FMCW radar sensors where the linearity of the VCO is an important design specification.

RTUIFR-10

A Multi-Standard Adaptive Image-Reject Downconverter

A. Tasic, S.-T. Lim, W. A. Serdijn and J. R. Long

Electronics Research Laboratory/DIMES, Delft University of Technology, The Netherlands

A multi-standard adaptive image-reject downconverter (oscillator and dual mixers) that satisfies the basic requirements of 2nd and 3rd generation wireless standards (i.e., DCS1800, W-CDMA, 802.11b, Bluetooth and DECT) is presented. The adaptivity between the standards is achieved by trading RF performance for current consumption, ranging from 9.9mA for the relaxed mode (2.4GHz DECT) to 20.2mA for the highest performance mode (1.8GHz DCS1800) of operation.

RTUIFR-11

High Frequency Noise Optimization of Sub-100nm MOSFETs Utilizing Three Dimensional TCAD Simulation

T. Tatsumi Sony Corporation

High frequency noise issues with scaled MOSFETs are calculated and analyzed for the purpose of structure optimization utilizing a three dimensional TCAD device simulator and following results have been revealed; for the transistors with a gate length less than 100nm , the induced gate noise becomes very sensitive to the gate width; the current concentration by the divot at the edge of the gate makes all of the channel noise, gate induced noise and NF_{min} worse.

RTUIFR-12

Low Frequency Spurs of VCO Due to Noise Propagation from Digital I/O's and their Effects on Performance of Bluetooth SoC

Shouhei kousai, Kenichi Agawa, Hiroki Ishikuro, Hideaki Majima, Hiroyuki Kobayashi, Daisuke Miyashita, Takahisa Yoshino, Youichi Hama, and Mototsugu Hamada, SoC Research and Development Center, Toshiba Corporation

This paper describes the effect of digital noise on RF circuits on the singlechip Bluetooth SoC. Low frequency components in the digital noise, generated by I/O circuits accessing to an external memory, are found to be converted to the phase noise as the spurs of voltage controlled oscillator (VCO). The spurs bring the performance degradation of wireless communications systems. To manage the gain of the VCO and the coupling coefficient shown to be a key to mitigate the performance degradations.

RTUIFR-13

A Broadband and Scalable Model for On-chip Inductors Incorporating Substrate and Conductor Loss Effects

J. C. Guo, T. Y. Tan, Dept. of Electronics Engineering, National Chiao Tung Univ., Hsinchu, Taiwan

A new T-model is developed to accurately simulate the broadband characteristics of on-Si-chip spiral inductors, up to 20GHz. The spiral coil and substrate RLC networks built in the model play a key role responsible for conductor loss and substrate loss in the wide-band regime, which cannot be accurately described by the conventional p-model. Good match with the measured S-parameters, $L(\omega)$, $\text{Re}(Z_{in}(\omega))$, and $Q(\omega)$ proves the proposed T-model. Besides the broadband feature, scalability is justified by the good match with a linear function of coil numbers for all model parameters employed in the RLC networks. The satisfactory scalability manifest themselves physical parameters rather than curve fitting. A parameter extraction flow is established through equivalent circuit analysis to enable automatic parameter extraction and optimization. This scalable inductor model will facilitate optimization design of on-chip inductor and the accuracy proven up to 20GHz can improve RF circuit simulation accuracy demanded by broadband design. Index Terms – Inductor, lossy substrate, broadband, scalable

RTUIFR-14

The Transformer Characteristic Resistance and Its Application to the Performance Analysis of Silicon Integrated Transformers

E. Ragonese, F. Carrara, T. Biondi*, A. Italia, A. Scuderi, and G. Palmisano, Università di Catania - Facoltà di Ingegneria - DIEES, Catania, Italia, *STMicroelectronics, Catania, Italia

In this paper a novel figure of merit for the rating of integrated transformers is presented. The proposed parameter provides a more reliable performance characterization compared to the insertion loss and maximum available gain, since it is inherently related to the maximization of the available output power in tuned load RF circuits. The new figure of merit is used to evaluate the effect of different substrate management approaches on the performance of silicon integrated transformers.

RTUIFR-15

CDMA2000 PCS/Cell SiGe HBT Load Insensitive Power Amplifiers

G. Berretta, D. Cristaudo, S. Scaccianoce, STMicroelectronics

A new design technique by an improved use of the load pull method for high efficiency and high linearity power amplifiers is proposed. Two SiGe HBT MMIC power amplifiers, which meet the CDMA2000-1X specifications under a 4:1 VSWR load, are integrated using this technique.

RTUIFR-16

An ESD Protected RFIC Power Amplifier Design

Swaminathan Muthukrishnan*, Jian Zhao**, George Studtmann** and Sanjay Raman*, * Wireless Microsystems Lab, Bradley Dept. of ECE, Virginia Tech, Blacksburg, VA, 24061, ** M/A-COM, Integrated Products Business Unit, M/A-COM, Roanoke, VA

This paper presents the development of Electrostatic Discharge (ESD) protection circuitry for a three-stage Power Amplifier (PA) designed for 1.9 GHz Digitally Enhanced Cordless Telephone (DECT) applications. Through careful RF and ESD circuit co-design, good RF performance and ESD immunity are achieved. The PA features a high gain of 26dB at an output power of 25dBm, which remained unaffected due to the inclusion of ESD circuitry. The circuit's Power Added Efficiency (PAE) is also relatively unaffected, remaining at around 43%. The circuit is fabricated using a commercial 0.5 μ m SiGe-HBT process. The design is capable of protecting the PA from \pm 4kV to +1.5kV Human Body Model (HBM) ESD stresses.

RTUIFR-17

High-Linearity and Temperature-Insensitive 2.4 GHz SiGe Power Amplifier with Dynamic-Bias Control

W.-C. Hua, H.-H. Lai, P.-T. Lin, C. W. Liu, T.-Y. Yang*, and G.-K. Ma*,
Department of Electrical Engineering and Graduate Institute of
Electronics Engineering, National Taiwan University, Taiwan, R. O. C.,
*SoC Technology Center, ITRI, Taiwan, R.O.C.

A high-linearity and temperature-insensitive 2.4 GHz power amplifier (PA) with dynamic-bias control is realized in a SiGe HBT technology with 0.9 μm emitter width. Due to the bias linearization, the PB1dBB of 27 dBm is only 0.5 dB smaller than PBsatB, which is the record low to the best of our knowledge. With simple temperature-insensitive bias, the total current deviations from the room temperature are smaller than 6% and 10% at the linear PBoutB (24/20 dBm) for 802.11b and 802.11g, respectively.

RTUIFR-18

A 131 GHz Push-push VCO in 90-nm CMOS Technology

P.-C. Huang, R.-C. Liu, H.-Y. Chang, C.-S. Lin, M.-F. Lei, H. Wang,
C.-Y. Su*, and C.-L. Chang*, National Taiwan University, *Taiwan
Semiconductor Manufacturing Company

A 131 GHz cross-coupled push-push voltage controlled oscillator (VCO) is realized in 90nm CMOS technology. It can be tuned from 129.8 to 132 GHz, with a constant phase noise of -108.4dBc/Hz at 10MHz offset. The oscillator provides a push-push output power of -15.2 dBm and a fundamental output power of +0.33 dBm, under core current of 20 mA from a 1-V supply voltage. Maximum push-push and fundamental output powers are -11.4 dBm and +2.1 dBm, respectively.

RTUIFR-19

A New Kind of CMOS High Frequency Oscillators

G. Petit (1,2), R. Kielbasa (1), and V. Petit (2), (1) SupÈlec, Gif-sur-Yvette, F-91192, France, gilles.petit@supelec.fr, (2) Thales Airborne Systems, Elancourt, F-78851, France

This paper presents a new 6.5GHz oscillator designed in a 0.5 μm SOS CMOS technology. First the classical method of design of CMOS integrated oscillators is analyzed. Its drawbacks in the case of an f_0 too closed to the f_t are pointed out. Thus a new structure that avoids these drawbacks is proposed. The layout particularities are presented in the case of a 8.5GHz fully integrated oscillator in the previous SOS technology that has an f_t of 35GHz. Measurements results are then given and analyzed.

RTUIFR-20

An integrated 1.5 V 6 GHz Q-enhanced LC CMOS Filter with Automatic Quality Factor Tuning Using Conductance Reference

S. Li, N. Stanic, K. Soumyanath*, Y. Tsividis, Columbia University,
*Intel Corporation

We report the design of an integrated 4th-order Q-enhanced LC bandpass filter with automatic Q tuning. The filter passband is centered at 6 GHz, and has a bandwidth of 100 MHz. The filter draws 15 mA from a 1.5 V supply, achieving a 1-dB compression point dynamic range of 43 dB, while the total output noise integrated over the passband is -70.5 dBm. The Q-tuning loop uses a replica resonator of those in the filter as a voltage-controlled oscillator, and a conductance reference, rather

RTUIFR-21

A 1.25Gbps Burst-Mode Receiver IC with Extended Dynamic Range

C.C. Chen, C.M. Tsai, D.U. Li, and L.R. Huang, SoC Technology Center, Industrial Technology Research Institute

A 1.25Gbps burst-mode optical receiver for Ethernet passive optical network is realized in a 0.35mm SiGe BiCMOS process. With dual-TIA topology, the sensitivity and overload of the receiver can be optimized independently. The measured results show a dynamic range of -28.4dBm to -1dBm and settling time less than 50ns.

RTUIFR-22

A Low-Power SiGe-HBT Merged LNA and Mixer for 5GHz Wireless-LAN Receivers

Corrado Carta, Werner Baechtold, Electromagnetic Fields and Microwave Electronics Laboratory (IFH), Swiss Federal Institute of Technology (ETH), Zurich, Switzerland

This paper presents the design, impl. and charact. of a monolithic im.-rej. merged lownoise ampl. and mix. Without pre-ampl., the circ. fulfill the specs for the RF front-end of a WLAN low-IF rec. compliant with the 5GHz standards. It consists of a transcend., which feeds the current signal into two mixing diff. pairs; two polyph. filters are used to gen. LO quad. signals and provide im.rej. Fabr. in BiCMOS ft 120GHz, Conv.gain/pow.cons. is the highest reported at 5-6GHz

RTUIFR-23

A 40-dBm OIP₃, 2-GHz Silicon Bipolar LNA

C. Motta*, G. Girlando*, A. Castorina*, G. Palmisano**,
*STMicroelectronics, **University of Catania

A 2 GHz silicon bipolar LNA, based on a cascode architecture, implementing input and output matching networks, and designed to simultaneously optimize matching, noise and linearity, is presented. The LNA exhibits a gain of 18 dB, a noise figure of 1.6 dB and an OIP₃ of +40 dBm, while consuming only 4 mA. To measure the linearity performance a non-conventional test-bench was developed. Statistical simulations and measurements were carried out on the LNA revealing a high sensitivity of the OIP₃ to process variations. A technique to restore the linearity performance is also described.

RTUIFR-24

Analytical Thermal Noise Model Suitable for Circuit Design Using Short-Channel MOSFETs

Jong Wook Jeon, Seyoung Kim, In Man Kang, Kwangsuk Han,
Hyungcheol Shin, Seoul National University

This paper proposes a new analytical noise model for short-channel MOSFETs which covers both the linear and the saturation regions. Both the channel thermal noise model and the gate-induced model are presented. The analytical equations for the noise parameters are also derived. Modeling results show an excellent agreement with the measured noise parameter data.

RTUIFR-25

A Multiphase Phase/Frequency Detector Based Frequency Synthesizer

V.Lagareste*, F.Badets*, Y.Deval**, J.B.Begueret** and D.Belot*,
* STMicroelectronics, DAIS, Central R&D, Crolles, France,
** IXL Laboratory, University Bordeaux 1, Bordeaux, France

This paper presents a Multiphase Phase/Frequency Detector (MPFD) for PLL based frequency synthesizer that shares the phase correction information N times in a period of RF step. The MPFD allows moving, providing a better rejection of the reference spurious tone and reducing the charge pump current without bandwidth and loop filter modification.

RTUIFR-26

Integrated 2.4 GHz Class-E CMOS Power Amplifier

V. Saari, P. Juurakko, J. Ryyanen, K. Halonen, Helsinki University of Technology, Electronic Circuit Design Laboratory

An integrated two-stage class-E power amplifier operating at the 2.4 GHz frequency range is described. The implemented power amplifier is capable of providing 21.3 dBm output power with power added efficiency of 40 % and gain of 14.3 dB at 2.4 GHz. The drain efficiency of the class-E power stage is 55 % at 21.3 dBm power. The power amplifier uses 3.3 V supply voltage and was fabricated with 0.18 μ m CMOS technology. The linear gain is 23.8 dB and the chip area 0.43 mm².

RTUIFR-27

A Low Phase Noise Quadrature LC VCO in CMOS Technology

B. Sze and C. Ho, VIA Technologies, Inc.

A quadrature LC VCO is designed and fabricated using standard 0.18 μ m CMOS process. The oscillation frequency can be tuned from 1400 to 1530 MHz through the 2-bit switch capacitor array. The measured phase noise is \sim 125.04 dBc/Hz at 600KHz offset from 1.5 GHz carrier. The measured harmonic distortion is below \sim 26dBc. The designed VCO has achieved the figure of merit (FOM) number of -185.4 dBc/Hz, which is the best among the compared VCOs with on-chip inductors using standard CMOS process.

RTUIFR-28

Non-Intrusive Testing Methodology for CMOS RF LNAs

J.Liobe, Y.Xiang, and M. Margala, University of Rochester

This paper proposes a non-intrusive testing methodology for CMOS RF LNAs using the gain of the LNA as a test response to examine the effects of a particular set of spot defect. The impact of four types of resistive bridging faults is analyzed on a practical LNA example. A performance threshold for each fault location is established. Initial results show that the use of the ADC is not only possible, but a highly accurate device for testing CMOS LNAs. A discussion about both the strengths and limitations of this approach is also included.

RTUIFR-29

A Circuit-Sensitive Methodology for Evaluating Substrate Noise

J. Liobe and K. Jenkins University of Rochester and IBM

This paper demonstrates a practical methodology for analyzing the impact of substrate noise in any sensitive circuit. From this methodology, a figure of merit (FOM) is proposed which can be used to compute the sensitivity of a circuit node to substrate noise. Simulations of a CMOS LNA prove the usefulness of this approach as a expeditious, yet effective means for determining the most substrate noise-sensitive portions of a circuit.

RTUIFR-30

A 2.4-GHz ISM-Transmitter IC with Novel Quadrature Clock Generation Technique for a Localization Application

G. Popken, P. Baureis*, M. Hartmann, H. Milosiu, H. Neubauer, F. Oehler, M. Peter, Fraunhofer Institute for Integrated Circuits, *University of Applied Sciences Würzburg-Schweinfurt

In this paper the design of a fully integrated 2.4 GHz ISM-band transmitter for a localization application will be presented. The signal path includes DAC, anti-alias filter, IQ modulator and power amplifier. The clock generation part comprises voltage controlled oscillator, phase-locked loop and a quadrature clock generator. A novel quadrature clock generation scheme is described in detail. It reduces phase errors significantly and avoids the VCO pulling

RTUIFR-31

A 2.5GHz Constant Envelope Phase shift Modulator for Low-Power Wireless Applications

X. Yang, C. Cao, J. Lin, K. K. O, J. Brewer, Department of Electrical and Computer Engineering, University of Florida

A low-power constant envelope phase shift modulator is presented. The circuit switches the phase of a constant amplitude carrier at output according to the input digital data. The operation is based on the digital circuit and therefore has very low power consumption. A modulator test chip was fabricated in a 0.18 μm Logic CMOS process. Experiment results verified the design principle of the modulator. The modulator consumes 2mA and is suitable for low power wireless applications like sensor network and personal area network. Since the design is implemented in digital circuit and has broadband frequency response, the modulator can be used at various wireless bands. In addition, the modulator can be used to generate different modulation schemes by controlling the phase and even amplitude digitally through a phasor-combining circuit. Therefore, the modulator can potentially be used for software defined radios.

RTUIFR-32

Fifth-Derivative Gaussian Pulse Generator for UWB System

H. Kim, Y. Joo, Electrical Engineering, Arizona State University

A noble pulse shaping method to design a ultra wideband (UWB) pulse generator is demonstrated with AMI 0.5- μm CMOS process in this paper. Four triangular pulse shapes are generated by CMOS digital circuit and combined at the output stage to generate the th-derivative Gaussian pulse. The output measured pulse width is 2.4ns and the average power consumption is 752 μW with 20MHz pulse repletion frequency (PRF).

RTUIFR-33

Dynamic Output Phase to Adaptively Improve the Linearity of Power Amplifier under Antenna Mismatch

A. Keerti and A. Pham, Microwave Microsystems Laboratory, University of California, Davis, CA

We present the development of a new adaptive circuit that preserves a power amplifier's (PA) performance under impedance mismatch caused at the antennas. The circuit includes a phase detector and a phase shifter that dynamically provide the optimal phase of the reflection coefficient at the output of the PA, to achieve the optimal performance under mismatch. Using this technique, the power amplifier maintains its performance close to that at 50 Ω , even under severe mismatch of VSWR 10:1.

RTUIFR-34

A Fully-Integrated Low Power Direct Conversion Transmitter with Fractional-N PLL using a Fast AFC Technique for CDMA Applications

M.W.Hwang, J.C. Lee, S.H. Beck, S. Yoo, K.H. Lim, H.S. Jung, T.H. Lee, K.L. Kim, G.H. Cho, and S. Han, Future Communications IC (FCI) Inc., Korea Advanced Institute of Science and Technology (KAIST).

This paper presents a fully integrated low power direct conversion transmitter IC for CDMA applications. To reduce the power consumption and reduce switching time, fractional-N PLL with VCO is integrated into transmitter IC and N-target algorithm is proposed to implement AFC. Total locking time is about 200 μ s including 80 μ s AFC lock time. Total current for -80dBm, -10dBm, and 8dBm output power are 27mA, 33mA, and 60mA, respectively. This chip is housed in a small 5mm x 5mm 32pin MFL package.

RTUIFR-35

A Low-Voltage, Low-Power, High dB-linear, and All CMOS Exponential V-I Conversion Circuit

Quoc-Hoang Duong and Sang-Gug Lee, RFME lab, Information and Communications University, 119-Mujro, Daejeon, Republic of Korea, 305-714.

Abstract- A very compact, all CMOS, exponential V-I conversion circuit was proposed, at low-voltage and low-power applications. The Taylor series expansion is used for realizing the exponential characteristics. A new technique to improve the dB-linear output current range has been introduced. Based on a 0.18 μ m CMOS process, the measurement results show a 44dB of output current range with very low current consumption of less than 0.17mA from 1.2V supply voltage. The proposed circuit can be used for the design of a low-voltage low-power analog and mixed-mode circuit such as variable gain amplifier (VGA) and automatic gain control (AGC) etc.

RTUIFR-36

CMOS Circular Geometry VCOs for Microwave Magnetic Field Generation

T. Yalcin, V. Sahin*, G. Boero, R. S. Popovic, Ecole Polytechnique Federale de Lausanne, *Decicon Inc.

In this paper we present 6 and 8 GHz CMOS VCOs capable of equi-phase microwave magnetic field generation for sensor applications. The VCOs are implemented in a balance-scale shaped circular-geometry structure, and prototyped using a standard 0.35 μ m CMOS technology. Both VCOs can generate magnetic fields of up to 1 mT within an on-chip 300 μ m diameter coil. Simulated phase noise is better than -120 dBc at 1 MHz. Measured frequency ranges are 1.1 and 0.6 GHz for the 6 and 8 GHz VCOs, respectively

RTUIFR-37

1.8 V, Variable Gain Transimpedance Amplifiers with Constant Damping Factor for Burst-Mode Optical Receiver

Wei-Zen Chen, Department of Electronics Engineering, National Chiao-Tung University, Ruei-Ming Gan*, STC, Industrial Technology Research Institute, Hsin-Chu, Taiwan*

This paper presents the design of high sensitivity and wide dynamic range transimpedance amplifiers for burst mode optical receiver. To achieve low noise and wide bandwidth design goals, both Butterworth and Bessel type TIAs are investigated, characterized, and the design techniques for noise optimization are proposed. The conversion gain of TIA is tunable with constant damping factor for wide dynamic range applications. Implemented in a 0.18 μm CMOS technologies, the TIAs provide 66 dBO in the high gain mode, 57 dBO in the low gain mode, and are capable of operating up to 4.5 Gbps. The measured sensitivity is up to -23.3dBm with 17 dB dynamic range at BER less than 10⁻¹². Operating under a 1.8 V supply, the power dissipations for Butterworth and Bessel type TIA are about 37.8 mW and 43.2 mW respectively. Chip size is 510 μm \times 520 μm .

RTUIFR-38

Design of CMOS Distributed Circuits for Multiband UWB Wireless Receivers

Payam Heydari, Denis Lin, Amin Shameli, Ahmad Yazdi, Department of Electrical Engineering and Computer Science, University of California, Irvine, CA 92697, U.S.A.

This paper presents the design and fabrication of an LNA and a mixer for the multiband UWB wireless receiver using distributed circuit topologies. First, the design of a 3-stage CMOS distributed LNA circuit consisting of three cascode cells is introduced. Next, the design of a 2-stage CMOS distributed mixer consisting of two single-balanced cells is presented. The LNA and mixer circuits are separately designed and fabricated in a 0.18 μm CMOS process.

PANEL SESSIONS

Day	Number	Time	Description
Mon	PMA	12:00pm - 1:20pm	CMOS PAs Step on the GaAs!
Tue	PTUA	12:00pm - 1:20pm	3G Handsets – Too Much Power in Your Hands?
Tue	PTUB	12:00pm - 1:20pm	Outsourcing: The impact on The Microwave Industry
Tue	PTUC	12:00pm - 1:20pm	RF/ Microwave/ Millimeter Wave Applications of Metamaterials
Wed	PWA	12:00pm - 1:20pm	CAD Tools for Microwave IC Design
Wed	PWB	12:00pm - 1:20pm	Trends for Future Deep Space Exploration
Wed	PWC	12:00pm - 1:20pm	Venture Capital and Entrepreneurial Opportunities in Microwaves
Thu	PTHA	12:00pm - 1:20pm	On the Potential Impact of Nanotechnology in the Microwave Field

RFIC SPONSORED PANEL SESSIONS (Details):

PMA: CMOS PAs Step on the GaAs!

Date & Time: Monday Lunchtime 12 Noon - 1:20pm

Location: Long Beach Convention Center – Grand Ballroom 1

Organizers: **Fazal Ali**, NOKIA
Mike Golio, RF Power Devices

Panelists:

- **Aditya Gupta**, Anadigics
- **Julio Costa**, RFMD
- **Pete Zampardi**, Skyworks
- **Ali Hajimiri**, Axiom/CalTech
- **Vikram Krishnamurty**, VT Silicon
- **TBD**

Abstract:

Research and development of RF/microwave power amplifiers based on CMOS technology has been ongoing for the last decade. In the past year, some CMOS based mobile phone product offerings have been demonstrated. Could this represent the beginning of the end for GaAs HBT and Si BJT technologies . . . or are CMOS PA's ultimately destined for the ash heap? Although the physical limitations of CMOS devices ensure that the incumbent (GaAs HBT and Silicon BJT) technologies will always be preferred for the mobile phone's power amplifier from a pure performance perspective, can the CMOS PA's offer other compelling advantages? The experts on our panel will discuss the performance (RF, thermal, robustness), process technology, cost, & maturity (levels of integration and packaging) related to CMOS power amplifier design and deployment. The panellists will also debate the specific future of GaAs HBT and CMOS power amplifiers for handset applications.

PTUA: 3G Handsets – Too Much Power in Your Hands?

Date & Time: Tuesday, June 14, 12 Noon - 1:20pm

Location: Hyatt Regency – Rooms A/B/C

Organizer: **Derek Shaeffer**, Aspendos Communications, Inc.

Panelists:

- **Aarno Parssinen** – Nokia
- **Bill Krenik**, Texas Instruments
- **Kamal Sahota**, Qualcomm
- **Larry Larson**, UCSD
- **Bernd Adler**, Infineon
- **Kevin Traylor**, Freescale
- **Tirdad Sowlati**, Skyworks Solutions

Abstract:

They're hot – literally. Third-generation cellular handsets still have a huge power problem compared to their more mature 2G counterparts. Closing the power gap is the focus of much industry effort. And, the multi-mode transceiver issues aren't getting any easier, now that we can expect to see any number of 'alternative' wireless interfaces popping up in cell phones in the future, many of which already have bandwidths far exceeding those of the current cellular standards. How will the power gap be closed in these advanced phones? What architectures can deliver the needed power reduction while solving the multi-mode problem? Will these be extensions of existing approaches, which have been highly optimized for 2G applications, or are we in for something entirely new? And, what technologies will be required to make this happen? Will we ever see the day when a single transceiver can handle these numerous standards?

RFIC AND NON RFIC SPONSORED TUTORIALS (Details):

TSA: Filter I: RF and Microwave Filter Design

Date & Time: Sunday, June 12; 8:00 AM to 5:00 PM
Location: Long Beach Convention Center, Room 203

Organizer: **H. Clark Bell**, HF Plus
Sponsors: MTT-8: Filters and Passive Components

TSB: BASIC RFIC BUILDING BLOCKS

Date & Time: Sunday, June 12; 8:00 AM to 5:00 PM
Location: Long Beach Convention Center, Room 102AB

Topics & Speakers:

- An Overview of Mobile Radios' RF System Architectures, W. Ali-Ahmad, Maxim
- Design of LNA, D. Shaeffer, Aspedos Communications
- Design of Up and Down converters, S. Kiaei, ASU
- Design of controlled oscillators, F. Svelto, University of Pavia
- Design of frequency synthesizers, M. Perrott, MIT
- Design of power amplifiers, R. Gupta, Berkana Wireless
- Design of duplexer, A. Cathelin, ST Microelectronics

Organizers: **Y. Deval**, IXL Lab
D. Shaeffer, Aspedos Communications
C. Rudell, Berkana Wireless

Sponsors: MTT-23: RFIC
2005 RFIC Symposium

This tutorial presents an overview of the design of integrated radiofrequency systems. The specific constraints of designing RFIC in low-cost silicon technologies will be highlighted. First, as a matter of introducing building blocks and their specifications, RF system architectures are described. Second, key building blocks are detailed, down to the transistor level. Device limitations due to the integration within silicon technologies are reviewed for each block. Last, reliability and test of highly integrated RF circuits are tackled.

TSC: MONOLITHIC DISTRIBUTED POWER MANAGEMENT FOR NEXT GENERATION WIRELESS APPLICATION

Date & Time: Sunday, June 12; 8:00 AM to 12:00 PM

Location: Long Beach Convention Center, Room 204

Topics & Speakers:

- Monolithic Power Management Circuits and Applications for RF Transceivers – Overview, S. Abedinpour, Freescale Inc.
- Power Management for High Spectral Purity RF Synthesizers, B. Bakkaloglu, Texas Instruments
- DC/DC converters and Noise Shaping Techniques for Switched-Mode DC/DC Converters for RF Transceivers, S. Kiaei, Connection One, ASU
- Design of Microfabricated Transformers and Inductors for High-frequency Power Conversion, A. Lotfi, Enpirion Inc.
- Adaptive Power Management for RF Power Amplifiers, G. Rincon-Mora, Georgia Institute of Technology, Analog Consortium

Organizers: **B. Bakkaloglu**, Texas Instruments

S. Abedinpour, Freescale Semiconductor

S. Kiaei, Connection One

Sponsors: MTT-23: RFIC

2005 RFIC Symposium

As CMOS technology is rapidly moving towards deep submicron gate lengths, there are several new challenges for the design of RF and analog circuits. One of the main challenges is the drastic reduction on the supply voltage which limits the linearity, dynamic range, and increases the supply ripple sensitivity of RF circuits. With the reduction of the RF supply voltage, noise, ripple and cross-coupling on the power supply is playing a dominant role in the transceiver noise budget. Specifically, synthesizer and reference oscillator phase noise, LNA and mixer noise figure and the adjacent channel requirement of the PA is heavily influenced by the supply noise and spurious content. With increasing drive towards higher level of integration, lower cost, and longer battery life in RF applications, there is a need for efficient monolithic DC-DC power converters. This workshop summarizes the topology tradeoffs that are involved in the implementation of monolithic distributed power management circuits for future generation portable wireless applications. RF supply regulators require high power density, high energy efficiency, low noise and ripple, high PSRR at a wide frequency range, small size, and low cost. The advantages and application areas of low-dropout linear, switched-mode DC-DC converters are examined in light of these requirements.

TMA: EMI/EMC FUNDAMENTALS FOR RF/MW ENGINEERS

Date & Time: Monday, June 13; 1:00 PM to 5:00 PM
Location: Long Beach Convention Center, Room 204

Organizers: **W. H. Cantrell**, Motorola & The Univ. of
Texas at Arlington
A. Mediano, The University of Zaragoza

Sponsors: MTT-17: HF, VHF, UHF Techniques

TFA: FERRITE, FERROELECTRIC, AND OTHER SPECIAL MATERIALS FOR MICROWAVE CONTROL

Date & Time: Friday, June 17; 8:00 AM to 5:00 PM
Location: Long Beach Convention Center, Room 201B

Organizers: **S. N. Stitzer**, Northrop Grumman Corp.
R. York, Agile Materials & Technologies
J. D. Adam, Northrop Grumman Corp.
L.E. Davis, University of Manchester

Sponsors: MTT-13: Ferrites and Ferroelectrics

TFB: SIGNAL INTEGRITY MODELING AND ANALYSIS

Date & Time: Friday, June 17; 8:00 AM to 5:00 PM
Location: Long Beach Convention Center, Room 203C

Organizers: **M. Abdulla**, Intel Corporation
O. M. Ramahi, University of Maryland at College Park

Sponsors: MTT-1: Computer-Aided Design
MTT-15: Microwave Field Theory

WORKSHOPS

Day	Number	Time	Description
Sun	WSA	8:00am-5:00pm	Competitiveness of Broadband Wireless Access (BWA) Systems
Sun	WSB	8:00am-5:00pm	Full CMOS Radio
Sun	WSC	8:00am-5:00pm	Advanced Technologies for Next Generation of RFIC
Sun	WSH	1:00pm-5:00pm	Noise Shaping Methods for RFIC Design
Sun	WSD	8:00am-5:00pm	Advanced System Solutions and Integration Technologies for High-Volume Wireless-LAN Applications
Sun	WSF	8:00am-12:00pm	Accuracy of System-Level Figures of Merit for Wireless Applications
Sun	WSG	8:00am-12:00pm	Circuit Characterization, Modeling and Testing: Can it Really Be Done Without Impedance Tune
Sun	WSE	8:00am-12:00pm	Impact of Component Modelling on Microwave and Millimetre Wave Circuit Performance
Sun	WSI	1:00pm-5:00pm	On-Wafer Microwave Measurements: State of the Art and Future Directions
Sun	WSJ	1:00pm-5:00pm	Practical Implementation of RF Power Amplifiers for Cellular Base Stations
Sun	WSK	1:00pm-5:00pm	Design Considerations and Tools for the System Level Design of RFICS
Sun	WSL	1:00pm-5:00pm	Multi-Band, Multi-Mode RFICS
Mon	WMA	8:00am-5:00pm	Application and Technology of High-Speed Analog to Digital Converters
Mon	WMB	8:00am-5:00pm	Filter II: Practical Aspects of Microwave Filter Design and Realization
Mon	WMC	8:00am-5:00pm	Advances in RF Power Amplifiers: Modeling, Design and Linearization
Mon	WMH	8:00am-5:00pm	Terahertz Radiation: Technology, Applications and Measurement Methods
Mon	WMD	8:00am-12:00pm	AM Noise in Modern Receivers
Mon	WMF	8:00am-12:00pm	Packaging and Interconnects for Microwave Photonics Applications
Mon	WMG	8:00am-12:00pm	Liquid Crystal Polymers for Microwave and Millimeter Wave Packaging
Mon	WME	8:00am-12:00pm	High Frequency Digital Backplane Interconnect Characterization and Design
Mon	WMI	1:00pm-5:00pm	New Developments in Low-Noise Frequency Sources
Mon	WMJ	1:00pm-5:00pm	Low Cost Packaging for Microwave and Millimeter-Wave Products

WORKSHOPS (continued)

Day	Number	Time	Description
Mon	WMK	1:00pm-5:00pm	Technology and Implementation of High Speed/GHz Digital Interconnections
Fri	WFA	8:00am-5:00pm	Physics, Theory, Fabrication and Applications of Microwave Metamaterials
Fri	WFB	8:00am-5:00pm	RF Aspects of Software Defined Radio (SDR)
Fri	WFC	8:00am-5:00pm	Advances in Automated Modeling and Microwave Design
Fri	WFD	8:00am-5:00pm	Advances in High-Efficiency Power Device and Circuit Technologies
Fri	WFE	8:00am-12:00pm	Recent Advances in RF Mems
Fri	WFF	8:00am-12:00pm	Very Large Microwave Arrays for Radio Astronomy and Space Communications
Fri	WFG	1:00pm-5:00pm	Rediscovering Circuit Design Techniques for Microwave Components, Circuits and Subsystems: The Efficiency and Power of EM/Circuit Codesign
Fri	WFH	1:00pm-5:00pm	See Through Wall Radars

RFIC SPONSORED WORKSHOPS (Details):

WSB: FULL CMOS RADIO

Date & Time: Sunday, June 12; 8:00 AM to 5:00 PM

Location: Long Beach Convention Center, Hyatt Regency B

Topics & Speakers:

- Impact of technology scaling on mixed signal design, C. Sodini, MIT
- Challenges in design of single chip radio for cellular communication systems, S. Embabi, Sirific.
- The future of RF CMOS modeling, A. Niknejad, UC Berkeley
- CMOS PAs, A. Hajimiri, Caltech.
- New dimensions in CMOS RF technologies, D. Ham, Harvard University.
- Full CMOS radio: Design issues and challenges, A. Rofougaran, Broadcomm.
- Bandwidth-Enhanced CMOS Fractional-N Synthesizers, I. Galton, UC San Diego.
- Future of MEMS in full CMOS radio, G. Rebeiz, UC San Diego.

Organizer: **W. Y. Ali-Ahmad**, Maxim Integrated Products
W. Khalil, Intel Corporation

Sponsors: MTT-23: RFIC
2005 RFIC Aymposium

As CMOS technology is scaling down, the question poses itself: What is the future of all-CMOS radio on a chip? The concept of full CMOS radio is an evolving reality, and the motivation for this workshop is to present key technical issues and put forward recommendations for future enabling technologies and design ideas. The workshop explores the impact of transistor and supply scaling on all-CMOS RF and mixed-signal circuits. The all-CMOS radio SoC (System-on-Chip) concept is tackled vs. the all-CMOS SiP (System-in-Package) concept with stress on design challenges and on integration and cost issues. The major topics addressed in this workshop include reducing substrate noise effects in all-CMOS radio chip, future RF CMOS modeling, digital calibration of Frac-N synthesizers and modulators, concepts of embedding high power CMOS PAs, power management circuits, and MEMS in full CMOS radio SoC.

WSC: ADVANCED TECHNOLOGIES FOR NEX GENERATION OF RFIC

Date & Time: Sunday, June 12; 8:00 AM to 5:00 PM

Location: Long Beach Convention Center, Room 103AB

Topics & Speakers:

- IProspects on Silicon CMOS for High frequency application, J. D. Alamo, MIT
- IBAW and MEMs above silicon for RF applications, P. Ancy, STMicroelectronics
- IBulk acoustic wave filters and new architectures for RF applications, C. Enz, CSEM
- IFBAR for RF applications, R. Ruby, Agilent
- IAdvanced technologies in order to cover future RF applications needs, M. H. Smith, Intel
- IBulk Acoustic Wave Filters for Mobile Cellular Communications, H. J. Timme, Infineon
- IImpact of new technologies for new RF systems, C. Nguyen, DARPA
- IFreescale's RF-IC Technologies - The Role of III-V and Si-based Devices in Advanced RF Applications, M. Huang, Motorola

Organizers: **D. Belot**, STMicroelectronics

Y. Deval, IXL lab

D. SAIAS, STMicroelectronics

Sponsors: MTT-23: RFIC

2005 RFIC Symposium

New technologies are currently emerging, which will dramatically impact the design of radiofrequency integrated circuits in a close future. Among them, the advent of Bulk Acoustic Wave devices (BAW) as well as Silicon On Insulator industrial processes (SOI) will undoubtedly open the way to a new era of RFIC System On Chip – assuming that the cost remain as low as possible and the reliability as high as possible. This workshop addresses different BAW technologies and approaches, emphasizing on RF functions for which this device cannot be overlooked. SOI technologies will be addressed too, for its influence on high frequencies as well as low-power consumption, and mixed-signal circuits. Finally, carbon nanotubes will be presented, as it might become an alternative to silicon transistors in the future. As CMOS technology is scaling down, the question poses itself: What is the future of all-CMOS radio on a chip? The concept of full CMOS radio is an evolving reality, and the motivation for this workshop is to present key technical issues and put forward recommendations for future enabling technologies and design ideas. The workshop explores the impact of transistor and supply scaling on all-CMOS RF and mixed-signal circuits. The all-CMOS radio SoC (System-on-Chip) concept is tackled vs. the all-CMOS SiP (System-in-Package) concept with stress on design challenges and on integration and cost issues. The major topics addressed in this workshop include reducing substrate noise effects in all-CMOS radio chip, future RF CMOS modeling, digital calibration of Frac-N synthesizers and modulators, concepts of embedding high power CMOS PAs, power management circuits, and MEMS in full CMOS radio SoC.

WSH: NOISE SHAPING METHODS FOR RFIC DESIGN

Date & Time: Sunday, June 12; 1:00 PM to 5:00 PM

Location: Long Beach Convention Center, Room 201B

Topics & Speakers:

- Overview of Transmit and Linear PA Up-converters, S. Kiaei, Connection One
- Fractional-N Frequency Synthesizers, I. Galton, UC San Diego,
- Polar Modulation methods for Power Amplifiers, Trinidad Sowlati, Skyworks,
- Algorithms and Amplifiers for Digital Generation of Microwave Signals with Time-Varying Envelope, P. Asbeck, J. Rode, I. Galton and L. Larson, aUC San Diego

Organizers: **B. Bakkaloglu**, Texas Instruments

S. Kiaei, Connection One

Sponsors: MTT-23: RFIC

2005 RFIC Aymposium

This workshop presents noise shaping and digital signal processing techniques for RF IC Design. The tutorials will cover fundamentals of modulation and various noise shaping techniques, development of Direct Digital Synthesis modulators and design of fractional-N synthesizers. Tradeoffs between phase noise and loop bandwidth in conventional fractional phase-locked loops will be analyzed and various techniques to cancel excess phase noise in modulated fractional-N controllers will be introduced. This workshop summarizes the topology tradeoffs that are involved in the implementation of various RF CMOS blocks utilizing the and noise shaping methodologies, and their application for future generation portable wireless systems. his workshop presents noise shaping and digital signal processing techniques for RF IC Design. The tutorials will cover fundamentals of modulation and various noise shaping techniques, development of Direct Digital Synthesis modulators and design of fractional-N synthesizers. Tradeoffs between phase noise and loop bandwidth in conventional fractional phase-locked loops will be analyzed and various techniques to cancel excess phase noise in modulated fractional-N controllers will be introduced. This workshop summarizes the topology tradeoffs that are involved in the implementation of various RF CMOS blocks utilizing the and noise shaping methodologies, and their application for future generation portable wireless systems.

WSD: ADVANCED SYSTEM SOLUTIONS AND INTEGRATION TECHNOLOGIES FOR HIGH-VOLUME WIRELESS-LAN APPLICATIONS

Date & Time: Sunday, June 12; 8:00 AM to 5:00 PM

Location: Long Beach Convention Center, Room 101AB

Topics & Speakers:

- MIMO WLAN Transceiver Concepts and its Implication on the FEM development, Avi Biran, Intel Corp
- Ultra-Compact WLAN FEMs for the High-Volume Wireless Mobile Market, Patric Heide, EPCOS AG
- RF Silicon Integrated Passives (RFIPDs) for WLAN Applications, C. H. Wang, Telephus
- Laminate-Based RF Integrated Passive Frontend Devices for WLAN Application, J. Chamberlin, JMD
- LTCC Front End Module for WLAN Application (IEEE 802.11a/b/g), S. Kemmochi, Hitachi Metals
- Small-size WLAN integrated modules, K. K. Kano and K. Kato
- FEMs for Mobile / Cellular Applications, B. Hemish and P. Huang, SiGe Semiconductor

Organizers: **Patric Heide**, EPCOS AG
Avi Biran, Intel Corporation
Clemens Ruppel, EPCOS AG

Sponsors: MTT-20: Wireless Communications
MTT-16: Microwave Systems
MTT-23: RF Integrated Circuits
2005 RFIC Symposium

The WLAN market demonstrated enormous growth rates in the last few years. Likewise the cellular phone market, the WLAN market has seen strong component cost reductions, with simultaneous increase in the complexity of WLAN radio transceivers - from single to multi-band / multi-mode solutions, coexistence with Bluetooth, novel cellular functions and, most recently - the realization of 802.11n and MIMO concepts. Apparently, the size of WLAN-radio transceiver RFIC and its adjacent FEM became a critical system-implementation factor. Wireless connectivity has become an embedded feature in mobile PCs, PDAs and smart phones, where, the number of functions per sq. mm is the limiting functionality factor. Very small WLAN RFICs with form factors compatible to CF and SD cards, memory sticks and USB-interfaces have been introduced in 2004. Highly-integrated FEM and single-chip radios have for the first time been applied to allow those innovative implementations. Most recently, the cellular industry has set the very challenging target of implementing a high-performance WLAN radio within 150 sq.mm (802.11g) and 250 sq.mm (802.11a + g) challenges. This will drive further the trend for higher integration levels, cost reduction, reliability and yield improvements.

WSK: DESIGN CONSIDERATIONS AND TOOLS FOR THE SYSTEM LEVEL DESIGN OF RFICS

Date & Time: Sunday, June 12; 1:00 PM to 5:00 PM
Location: Long Beach Convention Center, Room 102C

Topics & Speakers:

- Mixed-Signal Integrated Circuit Design Methodology and Challenges, M. Sunori, Matsushita Electric Industrial Co, Ltd.
- The RF Bottleneck in Wireless Design, J. Hartung, Cadence Design Systems, Inc.
- Early Verification of Emerging UWB and WMAN Radio Systems', T. Phillips, Agilent Technologies

Organizers: **A. Dengi**, Cadence Design Systems, Inc.
W. Geppert, Infineon Technologies

Sponsors: MTT-23: RFIC
2005 RFIC Symposium

The complexity of communication systems is increasing with each generation of communications standards, e.g., 802.11a-> b -> g, 2G -> 2.5G -> 3G, etc. With deep submicron technologies, a significant part of a communication system can now be integrated into one integrated circuit. Shrinking time-to-market requirements combined with the increasing complexity of integrated circuits have necessitated changes and improvements in IC design methodology and supporting design automation tools. System level simulation and verification, signal integrity analysis, unifying system level and circuit level design tools are some of the challenges. This workshop will present some of these design challenges and propose some methodology and design automation solutions for the next generation communications integrated circuits.

WSL: MULTI-BAND, MULTI-MODE RFICS

Date & Time: Sunday, June 12; 1:00 PM to 5:00 PM

Location: Long Beach Convention Center, Room 204

Topics & Speakers:

- Wideband front-end ICs and their compensation techniques, T. Nakagawa, NTT
- Multi-mode CMOS transceivers and architectures, T. Manku, Sirific Wireless Corporation
- Concurrent multiband RFICs, H. Hashemi, University of Southern California
- Switched multi-mode receiver ICs, J. Ryyänen, Helsinki University of Technology
- A broadband SiGe quadrature mixer for 0.8-5.2GHz wireless applications, N. Suematsu, Mitsubishi Electric

Organizers: **T. Nakagawa**, NTT

N. Suematsu, Mitsubishi Electric

Sponsors: MTT-23: RFIC

2005 RFIC Symposium

Wireless communications, including 2G and 3G cellular, 2.4- and 5-GHz wireless LAN, Bluetooth and GPS, have proliferated rapidly. These forms of communication will not be confined to a single system. In fact, one of the main user requirements is to be able to connect to networks anytime, anywhere using the most suitable wireless system of all the various wireless systems available, according to the situation. This broad requirement has led to a demand for multi-band and multi-mode transceiver ICs. Even though such transceivers feature both multi-band and multi-mode operations, they must be small and economical and have low power consumption. There are various integrated approaches to multi-band ICs, such as parallel RF paths, wideband circuits, multi-pass band circuits, tunable circuits and switching circuits.

This half-day workshop will review these and other techniques for achieving multi-band and multi-mode RFICs, and discuss what the right approach is, in the light of RF performance and cost, at present and in the future.

WFB: RF ASPECTS OF SOFTWARE DEFINED RADIO (SDR)

Date & Time: Friday, June 17; 8:00 AM to 5:00 PM

Location: Long Beach Convention Center, Room 101AB

Topics & Speakers:

- Regulatory issues: Spectrum pooling, D. Shrum
- Broadband antennas, S. Lindenmeier, Universität der Bundeswehr München
- Configurable RF Systems, J.-F. Luy, DaimlerChrysler
- Direct RF sampling, D. Akos, University of Colorado
- Frequency conversion processes in SDR front-ends, T. Mack, DaimlerChrysler
- Six port technology, K. Wu, University of Montreal
- Challenges for SDR – Transmitters, G. Fischer, Lucent Technologies.
- SDR and beamforming, J. Morton, University of Miami
- RF front-end and digital signal processing, M. Sliskovic, HarmanBecker

Organizers: **J.-F. Luy**, DaimlerChrysler

Y. T. J. Morton, University of Miami

Sponsors: MTT-9: Digital Signal Processing
2005 RFIC Symposium

Software Defined Radios require specific concentration of RF research and engineering work. The scope of this workshop is to discuss the most important RF aspects in this field. Regulatory issues may influence and will be influenced by the advance of SDRs. Broadband and multiband antennas will play an important role for the realization of SDRs with spectral adaptivity. In order to shift the digital signal processing parts as close as possible to the antenna the required RF components have to fulfil a number of requirements. Different schemes for the receiver architectures will be discussed as well as transmitter approaches. Presentations on SDR and beamforming and the relation between analog and digital aspects in SDRs will conclude the workshop.

REGISTRATION

REGISTRATION REQUIREMENTS

Registration fees are required of all participants, including session chairs, authors, workshop and panel session organizers and speakers.

ADVANCE REGISTRATION

All registrants who select the IEEE member rates will be required to produce their current IEEE membership cards upon check-in at the conference. Registrants who do not have their current IEEE membership cards at check-in will be charged nonmember rates.

Reduced rates are offered for advance registration when received by May 5, 2005. A registration form is available as an insert to this program. Each registrant must submit a separate form, with payment, to the address shown at the bottom of the registration form. If using a credit card, then fax and online registration is available. When mailing, please mail early to ensure receipt by the deadline; otherwise, on-site fees will apply.

Individual remittance must accompany the registration form and is payable in US dollars only. Personal checks drawn on US banks, traveler's checks, international money orders or credit cards (MasterCard, VISA or American Express) are accepted. Personal checks must be encoded at the bottom with the bank number, account number and check number. Bank drafts, wire transfers and cash are unacceptable and will be returned. Government or company purchase orders will not be accepted and will be returned.

GUEST REGISTRATIONS

To register your guest, include his or her name on your advance registration form. Guest badges will be included in the envelope that you will receive upon check-in. Onsite guest registration also will be available.

STUDENTS, RETIREES AND LIFE MEMBERS

Students, retirees and IEEE Life Members receive a substantial discount on the IMS registration fee. To qualify as a student, a registrant must be either a student member of IEEE or a full-time student carrying a course load of at least nine credit hours. A student identification card must be presented at check-in. ARFTG also provides discounts for students and retirees.

PRESS REGISTRATION

Credentialed press representatives are welcome to register on-site only, at the Exhibitor Counter, without cost. Press registrants will have access to technical sessions and exhibits. The Press Room is located in Room TBD.

ON-SITE REGISTRATION

On-site registration for all Microwave Week events will be available at the Long Beach Convention Center. Registration hours are:

Saturday, June 11	2:00pm - 6:00pm
Sunday, June 12	7:00am - 6:00pm
Monday, June 13	7:00am - 5:00pm
Tuesday, June 14	7:00am - 5:00pm
Wednesday, June 15	7:00am - 5:00pm
Thursday, June 16	7:00am - 3:00pm
Friday, June 17	7:00am - 9:00am

SOCIAL EVENTS

RFIC SYMPOSIUM RECEPTION:

Sunday evening, June 12th, is a highlight of RFIC technical activity and social festivities. **See Details Inside Front Cover**

MICROWAVE JOURNAL/MTT-S RECEPTION:

All Microwave Week attendees and exhibitors are invited to attend a reception hosted by Microwave Journal and MTT-S on Monday, June 13 from 6:00 to 8:00pm at the Aquarium of the Pacific on Shoreline Drive, two blocks from the convention center.

IEEE MTT WOMEN IN ENGINEERING RECEPTION:

The IEEE MTT Women in Engineering (WIE) committee will host a meeting and reception on Tuesday, June 14 from 5:30 to 7:00pm in the Hyatt Hotel. Meet and interact with professionals who share an interest in promoting the WIE forum.

HAM RADIO SOCIAL

All radio amateurs who are attending IMS2005 are cordially invited to a social gathering on Tuesday, June 14 from 6:00 to 9:00pm in the Hyatt Hotel.

INDUSTRY-HOSTED COCKTAIL RECEPTION:

Symposium exhibitors will host a cocktail reception on Wednesday, June 15 from 5:45 to 7:15pm at the Hyatt Regency Hotel. Complimentary beverage tickets will be included in the registration packages.

IEEE MTT-S AWARDS BANQUET:

The annual Awards Banquet will be held on Wednesday, June 15 from 7:30 to 10:00pm at the Hyatt Hotel. This evening will consist of an elegant dinner, awards presentation and entertainment. Major society awards will be presented at this event. The banquet is free of charge to the awardees.

IEEE MTT-S STUDENT AWARDS LUNCHEON:

Student Paper Awards, MTT graduate Fellowships and MTT Undergraduate Scholarships will be presented at the Student Awards Luncheon at noon, Thursday, June 16. The Luncheon is free of charge for all IMS2005 student paper finalists and their advisors.

TECHNICAL ATTENDEES BREAKFAST:

Monday-Thursday (June 13-16), at the LBCC from 7:00 to 9:00am. This breakfast is for all persons registered as technical participants in the IMS, RFIC or ARFTG (not open to those registered only as exhibitors or guests). IMS/RFIC/ARFTG badge required for admission.

TRANSPORTATION

Long Beach is part of the greater Los Angeles metropolitan area. It is located in Los Angeles county, about 25 miles south of the heart of the city of Los Angeles. With three interstates running through Long Beach, it is very easy to get to and from the city by car. Long Beach has its own airport and its own bus and taxi services. It is also served by the Los Angeles Metro light rail system. Downtown Long Beach is very friendly to pedestrians, and traveling local streets is easy with a good map.

There are three nearby airports and a total of five airports hosting all major domestic and international air carriers in the LA area.

- Long Beach Airport (airport code LGB): The Long Beach convention center and most conference hotels are located just 7 miles by ground transportation from the Long Beach airport. The Long Beach airport is served by Alaska Airlines, American Airlines, America West Airlines, and Jet Blue Airways. The airport offers taxi service and rental cars. www.longbeach.gov/airport
- Los Angeles International Airport (LAX): The world's fifth largest passenger airport is 23 miles northwest of the convention center by car. Over 50 commercial airlines fly in and out of LAX. The airport offers taxi and van services to Long Beach, rental cars, and Metro service via bus to light rail. www.lawa.org/lax
- John Wayne Airport (SNA): John Wayne Airport in Newport Beach is 25 miles from the convention center. it is served by 12 commercial airlines. The airport offers taxi and van service as well as rental cars. www.ocair.com
- Burbank Bob Hope (BUR) and Ontario (ONT) Airports are also located in the greater Los Angeles metropolitan areas.

The three closest airports offer van service to Long Beach. Contact Prime Time Shuttles (www.primetimeshuttle.com/SoCal.htm) at 800-733-8267 or Super Shuttle (www.supershuttle.com/htm/cities/lax/htm) at 800-258-3826 for rates and reservations. Service to Burbank and Ontario may be limited.

2005 GUEST PROGRAM

All tours will be made or cancelled based on advanced registration. We must have 30 advance registrations in order to operate most tours. Some tours have limited space. Please use advance registration if at all possible to avoid cancellation of the tours or the chance of missing a tour you want to go on. There may be slight changes in tour times, so please check the web page or at the hospitality suite.

Following are additional Web sites you may wish to access for viewing other activities and purchasing individual tickets to local entertainment and sporting events in the Long Beach area.

Long Beach Conventional & Visitors Bureau: <http://www.visitlongbeach.com>
 Disneyland: <http://disney.go.com/disneyland>
 Universal Studios: <http://www.universalstudios.com>
 Knotts Berry Farm: <http://www.knotts.com>
 Getty Museum: <http://www.getty.edu>
 Huntington Library & Botanical Gardens: <http://www.huntington.org>
 Aquarium of the Pacific: <http://www.aquariumofpacific.org>
 LACMA – Los Angeles County Museum of Art: <http://www.lacma.org>
 Page Museum – La Brea Tar Pits: <http://www.tarpits.org>
 Long Beach Museum of Art: <http://www.lbma.org>
 Long Beach Museum of Latin American Art: <http://www.molaa.com>

The Hospitality Suite for RFIC/IMS2005 attendee guests will be located in a private Concierge Lounge in the Hyatt Hotel. Guest badges will be required. The suite will be open as follows:

Sun, June 12, 2005 11:30am - 5:30pm
 Mon-Thu, June 13-16, 2005 7:00am - 4:30pm
 Fri, June 17, 2005 7:00am - 12:30pm

IMS steering committee members will be available for guest assistance in the suite. In the suite, guest may enjoy a daily continental breakfast and afternoon refreshment. Courtesy computers for EMAIL use will be available on site for adult guests. The guided tours will be leaving from the Hyatt lobby.

TOURS

Getty Museum Tour Sunday, June 12, 2005
 \$55 pp (advance registration) Noon - 5:00pm
 \$65 pp (on-site registration) *Hosted by Access California*

A Day in San Juan Capistrano Monday, June 13, 2005
 \$75 pp (advance registration) 9:00am - 3:30pm
 \$90 pp (on-site registration) *Hosted by Access California*

Pasadena and the Huntington Tuesday, June 14, 2005
 \$75 pp (advance registration) 9:00am - 3:00pm
 \$90 pp (on-site registration) *Hosted by Access California*

Exploring Long Beach Wednesday, June 15, 2005
 \$50 pp (advance registration) 9:00am - 3:00pm
 \$60 pp (on-site registration) *Hosted by Access California*

Long Beach Multi-Cultural Tour Thursday, June 16, 2005
 \$60 pp (advance registration) 9:00am - 3:00pm
 \$70 pp (on-site registration) *Hosted by Access California*

Catalina Island Trip Thursday, June 16, 2005
 \$65 pp (advance registration) 9:00am - 5:00pm
 \$80 pp (on-site registration - if available)
Hosted by the Steering Committee

Golf Outing Friday, June 17, 2005
 \$70 pp (advance registration only) 7:30am - 1:30pm
Hosted by the Steering Committee