The 2006 RFIC Symposium will be held in San Francisco, CA on June 11-13, 2006 in conjunction with the IEEE MTT-S International Microwave Symposium. It opens Microwave Week 2006, the largest world-wide RF/Microwave meeting of the year.

The RFIC Symposium brings focus to the technical accomplishments in RF systems, circuit, device and packaging technologies for mobile phones, wireless communication systems, broadband access modems, radar systems and intelligent transport systems.

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Message from the General Chairman

Stephan Heinen

Welcome to the 2006 RFIC Symposium! Again this year, the RFIC Symposium continues to build upon its heritage as one of the foremost IEEE technical conferences dedicated to the latest innovations in RFIC development of wireless and wire line communication IC's, with an exciting technical program. Running in conjunction with the International Microwave Symposium and Exhibit, the RFIC Symposium adds to the excitement of the microwave week with three days focused exclusively on RFIC technology and innovation. The symposium begins on Sunday June 11th with tutorials and workshops focused on RFIC technology, design, and systems. The RFIC Plenary Session starts at 5:30 pm on Sunday June 11th, following the workshops. It will be held in the Moscone Convention Center and opens the formal technical program. The Plenary Session will feature three distinguished speakers from industry, Mr. Stefan Wolff from Infineon Technolgies, Dr. Arogyaswami Paulraj from Beceem Communications, and Mr. Kent Heath from Freescale Semiconductor. These three renowned guests will share their views on the future direction of wireless and mobile communications IC's and systems. The RFIC reception begins immediately after the plenary, making Sunday evening a highlight of both technical activity and social festivities. This highly attended, enjoyable social event allows attendees to meet with old friends, catch-up on the latest events and interact with professionals in the wireless community.

The technical program continues on Monday and Tuesday with oral paper presentations, panel sessions, and an interactive forum. A panel session during lunch on Monday features a distinguished list of panelists discussing the subject '4G : Do we really need 1 Gits/s?'.

On Tuesday, a lunch panel session titled, "SoC vs. SiP : Dollars & Sense" includes another distinguished set of panelists discussing this high-interest topic. The interactive forum begins on Tuesday afternoon and is an excellent opportunity for attendees to meet authors and discuss their presentations in detail. The RFIC Symposium concludes on Tuesday allowing participants to attend the IMS and ARFTG as well as plenty of time to visit the exhibit hall.

Stefan Heinen
General Chairman
2006 IEEE RFIC Symposium

Message from the Technical Program Committee Chairmen

Luciano Boglione

Jenshan Lin

On behalf of the Technical Program Committee, welcome to the 2006 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. The RFIC Symposium is a leading edge IEEE technical conference dedicated to the advancement of integrated circuits and sub-systems for RF, wireless, broadband communications, and many other emerging applications. The RFIC Symposium will be held in San Francisco, CA, from June 11th to June 13th, 2006. The RFIC activities begin on Sunday, June 11th with workshops and tutorials addressing RF technology, design and integration, at both system and circuit level. The Plenary Session will be held on Sunday evening, right after the workshops. Three leading experts will share their own views during Sunday evening plenary session: Stefan Wolff, Vice President RF-Engines, Infineon Technologies, will talk about "RF-modems, the real application for RF CMOS"; then, Kent Heath, Director, Cellular Operations, Radio Products Division, Freescale Semiconductors, will discuss "Architectural implications of multimode, multiband cellular radios"; finally, Arogyaswami Paulraj, Founder and Chief Technology Officer, Beceem Communications, Professor, Stanford University, will speak about "Multiple antenna technology in mobile broadband - new challenges for RF designers". The RFIC reception will follow the plenary session to allow for everyone to relax and discuss the industry outlook among friends. The regular technical program takes place on Monday and Tuesday featuring invited and submitted technical papers. A panel session entitled "4G : Do we really need 1 Gbits/s?" will take place during lunch on Monday and have panelists from both industry and academia offer their views on the challenges ahead. Another panel session on Tuesday, "SoC vs. SiP : Dollars & Sense," is posed to allow for many interactive discussions with the audience! The interactive forum on Tuesday afternoon also gives attendees a further opportunity to meet one-on-one with authors. In all, the RFIC 2006 Symposium features 20 technical sessions, an interactive forum, 130 presentations, 13 workshops and tutorials, and 2 panel sessions. The interest in RFIC technology, and the venue offered by the Symposium to showcase the latest advancements, continues to be the venue of choice for both industry and academia to meet, discuss results and exchange ideas. The 2006 Technical Program Committee keeps working diligently toward the goal of strengthening the technical quality and scope of the program, while maintaining and improving the legacy left by the previous Symposia. This would not be possible without keeping the interest of professionals like you and gaining the trust of all the authors who submitted their work to the RFIC Symposium.

We hope you enjoy the 2006 RFIC Symposium!

Luciano Boglione and Jenshan Lin
Technical Program Committee Co-Chairs
2006 IEEE RFIC Symposium

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RFIC Schedule 2006

The RFIC Symposium will be held in the San Francisco Convention Center (SFCC – Moscone Center). The headquarters hotel is the SF Marriott which is close by. The RFIC Plenary and Reception will be held on Sunday June 11 at the SFCC.

The RFIC Symposium is held in conjunction with the International Microwave Symposium (IMS). Attendees of the RFIC Symposium are invited to attend the IMS Plenary Session on Tuesday June 13 and MTT Social Events.

Saturday June 10, 2006

2:00pm - 6:00pm	Registration – SFCC

Sunday June 11, 2006

7:00am - 6:00pm	Registration – SFCC
8:00am - 5:00pm	Workshops – SFCC
8:00am - 5:00pm	Tutorials – SFCC
5:30pm - 7:00pm	Plenary – SFCC Esplanade – Room 307-310
7:00pm - 9:00pm	RFIC Reception SFCC Esplanade Level

Monday June 12, 2006

7:00pm - 5:00pm	Registration – SFCC
7:00am - 8:00am	Speakers Breakfast SFCC East Mezzanine – Rooms 232 & 234
7:00am - 8:00am	Registered Attendee Breakfast SFCC – South Lobby
7:00am - 5:00pm	Speakers Preparation SFCC East Mezzanine – Rooms 203
8:00am - 9:40am	RFIC Oral Technical Sessions SFCC – See Listings
9:40am - 10:10am	Break – SFCC
10:10am - 11:50am	RFIC Oral Technical Sessions SFCC – See Listings
11:50am - 1:20pm	RFIC Panel – SFCC
1:20pm - 3:00pm	RFIC Oral Technical Sessions SFCC – See Listings
3:00pm - 3:30pm	Break – SFCC
3:30pm - 5:10pm	RFIC Oral Technical Sessions SFCC – See Listings
6:00pm - 8:00pm	Microwave Journal Reception Yerba Buena Gardens

Tuesday June 13, 2006

7:00am - 5:00pm	Registration – SFCC
7:00am - 8:00am	Speakers Breakfast SFCC East Mezzanine – Rooms 232 & 234
7:00am - 8:00am	Registered Attendee Breakfast SFCC – South Lobby
7:00am - 5:00pm	Speakers Preparation SFCC East Mezzanine – Rooms 203
8:00am - 9:40am	RFIC Oral Sessions SFCC – See Listings
9:40am - 10:10am	Break – SFCC Exhibits Area
10:10am - 11:50pm	MTT Plenary Session SFCC Esplanade – Room 307-310
11:50am - 1:20pm	RFIC Panel –SFCC
1:30pm - 4:30pm	RFIC Interactive Forum SFCC Gateway Ballroom – Room 103 & 104

Sunday, June 11, 2006 – 5:30 PM
SFCC – Room 307-310
Session RSU5A: RFIC Plenary

Session Chair: Stefan Heinen, RWTH Aachen University
Session Co,Chairs: Luciano Boglione, IECi and
Jenshan Lin, University of Florida

5:30PM	Welcome message from General and TPC Chairs, Announcement of Student Paper Awards
5:45PM	**RSU5A-1:** RF-Modems the Real Application for RF-CMOS, Stefan Wolff, Infineon Technologies
6:10PM	**RSU5A-2:** Multiple Antenna Technology in Mobile-Broadband – New Challenges for RF Designers, Arogyaswami Paulraj, Stanford, University
6:35PM	**RSU5A-3:** Architectural Implications of Multimode Cellular Radios, Kent Heath, Freescale Semiconductors

Plenary #1 - RF-Modems the Real Application for RF CMOS

by Stefan Wolff
Vice President RF-Engines
Infineon Technologies

Over the last decade wireless connectivity has become an integral and essential part of our life. The plain mobile phone of the early nineties has involved in mobile multimedia terminal. Consumers are demanding cell phones providing a comprehensive set of advanced features enabling voice, data and video services. Handset manufacturer have to accommodate their products to fast changing market requirements. The semiconductor supplier has to provide a cost effective and flexible platform, which enables the handset manufacturers to differentiate their products quickly and still maintaining a low development effort.

The vast majority of today's cell phones require at least a multiband radio. In the near future multimode multiband 2G and 3G operation will be a part of the main stream products including wireless LAN, Bluetooth®, GPS and DVB-H as well. Infineon Technologies has focussed its RF expertise on providing the next wave of highly integrated, high performance and easy to use RF CMOS radio subsystems. Infineon Technologies demonstrates the maturity of RF CMOS with respect to RF performance by producing e.g. a six-band WCDMA / UMTS transceiver. The RF CMOS capability enabled the world first single chip cell phone: EGold-Radio. RF-modems will be the next leap in the integration level. These RF-SoCs will simplify the handset development process by separating the radio hardware as well as the protocol stack from the application layer.

About Stefan Wolff:

Stefan Wolff is Vice president of Infineon Technologies overseeing the company's Cellular RF Engine business unit. Since the early nineties he is involved in RF IC business. After his studies he started his career at Robert Bosch group as RF engineer for Mobile Phones. Later he joined Siemens Semiconductor, where he was responsible for the marketing of RF ICs. Prior to joining Infineon Technologies, Mr. Wolff was heading the San Diego RF design centre of Siemens Mobile Phones.

Plenary #2 -: Architectural Implications of Multimode, Multiband Cellular Radios

by Kent Heath
Director, Cellular Operations
Radio Products Division
Freescale Semiconductors

With the industry trending toward high levels of integration and multiple radio technologies in a single RF lineup, Mr. Heath will present how the industry is addressing these issues. Combinations of System-on-Chip(SoC)- and System-in-Package(SiP)-level integration may be employed to meet the accelerating cost and size reduction needs of OEMs and carriers.

In the RF realm there are proponents of various technological approaches to these industry challenges. Different groups favor various approaches ranging from elaborate III-V technologies to SiGe-based methodologies, BiCMOS nodes and RFCMOS-based solutions. Some of these technologies are being proposed as single-chip solutions while many are leaning toward combinational approaches using various platforms for SiP-level integration. Mr. Heath will address the various approaches available and the potential implications to the mobile communications industry.

About Kent Heath:

Kent Heath is the director of cellular operations for Freescale's Radio Products Division. He joined Freescale Semiconductor in March of 2004 as director of the Analog Cellular IC business unit and was division strategy manager for the Radio Products Division based in Tempe, Arizona. He has responsibility for power management and user interface ICs, RF transceivers, power amplifiers, RF subsystems and DVB-H components targeted for the cellular handset market. Prior to joining Freescale, Kent was at Skyworks Semiconductor as senior director of strategy and business development for the RF Solutions Division from 2000-04, as director of Motorola Semiconductor's Wireless Subscriber Systems Group (WSSG) in Japan from 1197-2000 and at other engineering management positions at Xerox, Genisco Technology, and LectroMagnetics Inc., before coming to work for Motorola in 1991. Kent is a BSEE and MBA graduate from Southern Methodist University in Dallas. He has been a member of Semiconductor Industry Association in Japan (SIAJ), the Society of Mechanical Engineers (SME), and has been an active member of the Institute of Electrical and Electronic Engineers (IEEE) for over 20 years.

Plenary #3 – Multiple Antenna Technology in Mobile Broadband – New Challenges for RF Designers

by Arogyaswami Paulraj
Founder and Chief Technology Officer
Beceem Communications Professor
Stanford University

Multiple antenna wireless has emerged as a key technology that significantly improves coverage and throughput. Multiple input - multiple output (MIMO) is a configuration that uses multiple antennas at both ends of the link. This talk focuses on MIMO in mobile broadband. We begin with a survey of mobile broadband applications, markets and standards with special reference to multiple antenna technology. We describe the typical design of a next generation mobile broadband system that uses MIMO-OFDMA and highlight design areas that are impacted by MIMO. We then quantify the performance enhancement offered by multiple antennas in mobile broadband. Finally, we discuss RF design challenges related to multiple antennas at both terminals and base stations. We address mutual coupling and its impact of RF performance, transmit-receive RF calibration necessary for the transmitter to learn the channel, RF power drain and power management by controlling the number of active RF chains, and PAPR reduction. We end with a survey of emerging multiple antenna RF products.

About Arogyaswami Paluraj:

Dr. Arogyaswami Paulraj is a founder and Chief Technology Officer for Beceem Communications. He is also a Professor at the Dept. of Elect. Engineering, Stanford University, where, he supervises the Smart Antennas Research Group. This group works on applications of space-time wireless communications and has developed many key fundamentals in this new field as well as helped shape a worldwide research and development focus onto this technology. Paulraj has won several awards for his engineering and research contributions. Most recently he was awarded the IEEE SP Society Technical Achievement Award 2003. He is the author of over 300 research papers, a textbook on wireless communications, and holds 24 patents. Paulraj is a Fellow of the IEEE and a Member of the Indian National Academy of Engineering.

Monday June 12, 2006
8:00 AM
SFCC – Room 307-310
Session RMO1A: Cellular ICs I

Chair: Fazal Ali, Qualcomm
Co-Chair: Didier Belot, ST Microlectronics

RMO1A-1 8:00 AM
Tri-mode Integrated Receiver for GPS, GSM 1800, and WCDMA

N. Darbanian*, S. Farahani*, S. Kiaei**, B. Bakkaloglu**, M. H. Smith***, *Freescale Semiconductor Inc., **Arizona State University, ***Amalfi Semiconductor Inc.

A fully integrated direct conversion tri-mode receiver compliant with Global Positioning System (GPS), GSM1800, and WCDMA is presented. The configurable receiver consists of a wide band Low Noise Amplifier with an on-chip matching network, Gilbert-cell mxers, and dynamically reconfigurable gm-C base-band filters. The RF and analog blocks occupy 2.28 mm2 in 0.18um SiGe technology. The measurement results show Noise Figure as low as 3.2 dB for GPS and IIP3 of -18 dBm.

RMO1A-2 8:20 AM
A Low Power Low Noise Figure GPS/GALILEO Front-End for Handheld Applications in a 0.35um SiGe Process

R. Berenguer*, J. Mendizabal*, U. Alvarado*, D. Valderas*, A. García-Alonso**, *Centro de Estudios e Investigaciones de Gipuzcoa (CEIT), **TECNUN - University of Navarra

A highly integrated, low power GALILEO/GPS front-end for the new generation of positioning services has been designed using a 0.35um SiGe process. It has been implemented using a 6MHz bandwidth low IF architecture whose IF frequency is 4.092MHz. The fron-end exhibits a voltage gain of 103dB and presents a SSB NF of 3.7dB which makes it suitable for high sensitivity applications. The achieved power consumption is only 62mW from a 3V voltage supply with no compromise with performance.

RMO1A-3 8:40 AM
A WCDMA, GSM/GPRS/EDGE Receiver Front End without Interstage SAW Filter

Naveen Yanduru, Shanthi Bhagavatheeswaran, Chien-Chung Chen, Fikret Dulger, Sher Jiun Fang, Danielle Griffith, Yo-Chuol Ho, Kah Mun Low, Radio Design, Wireless Terminal Business Unit, Texas Instruments, Dallas, TX.

A dual mode RF receiver for DCS band in 90nm CMOS is presented. The receiver uses direct conversion for WCDMA and uses 100kHz low IF for GSM/GPRS/EDGE (GGE). The receiver does not use an interstage SAW filter between LNA and mixer. The mixer stage is folowed by a variable gain amplifier. Two times LO clock is provided from external source and a divide by two is used to generate quadrature clocks. The receiver has a NF of 2.9dB and meets all the out of band and in band linearity requirements.

RMO1A-4 9:00 AM
A 1-to-4 Channel Receiver for WCDMA Base-Station Applications

T. Tikka, J. Mustola, V. Saari, J. Ryynanen, M. Hotti, J. Jussila*, K. Halonen, Electronic Circuit Design Laboratory, Helsinki University of Technology, *Nokia Research Center

A base-station receiver, which is capable of receiving from one to four adjacent WCDMA channels, is described in this paper. The receiver is designed to drive a high-resolution A/D converters and it can be used as a direct-conversion receiver or as an lo-IF receiver in WCDMA bands I-III. The low-IF NF is 2.7 / 3.0 dB for the channels centered at 7.5 MHz and 2.5 MHz, respectively. The measured IIP3 of the receiver varies from -10 dBm to -8 dBm depending on the number of the received channels.

RMO1A-5 9:20 AM Invited
Evolution of a Software-Defined Radio Receiver's RF Front-End

A. A. Abidi, University of California, Los Angeles

Several techniques have evolved to enable a functional, low power CMOS software-defined radio receiver, that can tune any channel bandwidth at carrier frequencies from 800 MHz to 5 GHz. Key are clock programmable filters that assume the role of fixed RF refilters, and a method to sample narrowband signals immersed in a wide band of unwanted channels. The receiver handles all known blockers, and needs milliwatt A/D converters.

Monday June 12, 2006
8:00 AM
SFCC – Room 305
Session RMO1B: Frequency Generation

Chair: Ting-Ping Liu, Winbond Electronics - China
Co-Chair: Stephen Dow, ON Semiconductor

RMO1B-1 8:00 AM Invited

Taming Electrical Solitons: A New Direction in Picosecond Electronics

D. S. Ricketts, X. Li, and D. Ham, Harvard University, Cambridge MA 02138

Invited Paper The paper reviews the first electrical soliton oscillator, which self-generates a periodic, stable train of electrical soliton pulses. The soliton oscillator, which has been historically difficult to realize due to the soliton's instabilityrone dynamics, was made possible by combining the well-known nonlinear transmission line supporting electrical soliton propagation with an amplifier that \tames'' the instability-prone soliton dynamics on the nonlinear line.

RMO1B-2 8:20 AM

A 5GHz Above-IC FBAR Low Phase Noise Balanced Oscillator

M. Aissi*, E. Tournier*, M. -A, Dubois**, C. Billard***, and R. Plana*, *LAAS-CNRS, **CESM, ***CEA-LETI.

In this paper, a 5GHz FBAR banlanced oscillator is presented. The FBAR resonator was integrated directly above the 0.35um BiCMOS IC using surface micromachining. The use of the balanced configuration allows dividing by two the electrodes resistance of th FBAR. Therefore, better phase noise is obtained comparatively to the single ended version. The measured phase noise is -121dBc/Hz at 100kHz from 5.46GHz carrier frequency.

RMO1B-3 8:40 AM

A 17 dBm 64 GHz Voltage Controlled Oscillator with Power Amplifier in a 0.13 um SiGe BiCMOS TECHNOLOGY

Brian Welch, Ullrich Pfeiffer, IBM Thomas J. Watson Research Center

A 64GHz voltage controlled oscillator with power amplifier is presented. It uses an LC type oscillator with a capacitively degenerated negative resistance core, and a class AB power amplifier to output 17dBm of power with a phase noise of – 100 dBc/Hz (at 600 KHz). The stand alone oscillator delivers 5 dBm of output power (8 dBm balanced) with phase noise of between -95 dBc/Hz and – 100 dBc/Hz (at 600 KHz offset) and 2GHz tuning range. Separate voltage rails of 4V, 2V, and 1V are provided for the two stages of buffering and core, respectively, for a total power consumption of 130 mW. The PA is a class-AB push-pull amplifier made from two unbalanced cascode amplifiers with 15 dB power gain and 17 dBm saturated output power. The PA operates off the same 4V rail as the VCO buffer, consuming up to 500 mW of power for power added efficiencies of between 6-10%.

RMO1B-4 9:00 AM

Differential VCO and Passive Frequency Doubler in 0.18um CMOS for 24GHz Applications

D. Ozis, N. M. Neihart, D. J. Allstot, University of Washington, Seattle, WA, 98195

Circuits for generating a 24GHz LO signal from both a 12GHz VCO cascaded with a 2X passive mixer and a standalone 24GHz VCO are compared. The 24GHz designs exhibit equivalent phase noise, but the use of the passive mixer enables a 4X reduction in power cnsumption and a 2X increase in tuning range in comparison to the standalone VCO. The VCO/mixer combination shows a phase noise of -99.94dBc/Hz @1MHz offset from the 25.1GHz carrier, 12% tuning range, 11mW of power consumption in 0.18um CMOS.

RMO1B-5 9:20 AM

A 2.4-GHz Sub-mW Frequency Source with Current-Reused Frequency Multiplier

Taeksang Song, Hyoung-Seok Oh, Euisik Yoon*, Songcheol Hong, Korea Advanced Institute of Science and Technology (KAIST), *University of Minnesota

A fully integrated 2.4 GHz low-power frequency source including a 1.2 GHz VCO and a current-reused frequency multiplier is fabricated in 0.18-um CMOS process. The proposed frequency source tunes from 2.22 GHz to 2.45 GHz by changing control bias from 0 Vto 0.7V, and achieves a phase noise of -115.83 dBc/Hz at 1 MHz offset from a 2.2 GHz carrier frequency while drawing only 840 uA bias current (490 uA for a 1.2 GHz VCO and 350 uA for the frequency multiplier) from low supply voltage of 0.7 V.

Monday June 12, 2006
8:00 AM
SFCC – Room 306
Session RMO1C: UWB LNAs

Chair: Albert Jerng, MIT
Co-Chair: Kirk Ashby, Microtune

RMO1C-1 8:00 AM

A 1.2 V Reactive-Feedback 3.1-10.6GHz Ultrawideband Low-Noise Amplifier in 0.13um CMOS

M.T. Reiha, J.R. Long, J.J. Pekarik*, Delft University of Technology, *IBM Microelectronics

A 15.1dB gain, 2.1dB noise figure (min.), low-noise amplifier (LNA) fabricated in 0.13um CMOS is designed that covers the entire 3.1-10.6GHz UWB. Noise figure variation across the band is limited to ±0.43dB. Reactive feedback reduces the noise figure, stbilizes the gain, and sets the terminal impedances over the prescribed bandwidth. Bias current-reuse is used to limit power consumption of the 0.87mm2 IC to 9mW from a 1.2V supply.

RMO1C-2 8:20 AM

A 1.8-3.1 dB Noise Figure (3-10 GHz) SiGe HBT LNA For UWB Applications

Y. Lu, R. Krithivasan, W.-M.L. Kuo, and J.D. Cressler, School of Electrical and Computer Engineering, Georgia Institute of Technology

We present the design and implementation of an ultrawideband (UWB) SiGe HBT LNA for use in UWB systems. The use of a shunt base-emitter capacitor and weak shunt resistive feedback in a cascode amplifier with inductive degeneration significantly improves he input bandwidth of the LNA, and allows very low noise figure to be achieved simultaneously. The LNA exhibits a noise figure of 1.8-3.1 dB across 3.0-10.0 GHz, and operates off a 3.3 V supply with a total power consumption of 26 mW.

RMO1C-3 8:40 AM

A CMOS 3.1-10.6GHz UWB LNA Employing Stagger-compensated Series Peaking

S. Shekhar, X. Li*, D.J. Allstot, University of Washington, Seattle. *Qualcomm, Inc.

A fully-integrated common-gate UWB LNA employs a stagger-compensated series peaking technique to extend bandwidth, and a capacitor cross-coupled gm-boosting technique to reduce NF and power. For two versions in 0.18mm CMOS, measured BW extension factors re 4.1X and 4.9X, -3dB bandwidths are 1.3-10.7GHz and 1.3-12.3GHz, NF are 4.4dB and 4.6dB, peak S21 are 8.5dB and 8.2dB, and peak IIP3 are 8.3dBm and 9.1dBm, respectively. Each differential LNA draws 2.5mA from 1.8V.

RMO1C-4 9:00 AM

3~11-GHz CMOS UWB LNA Using Dual Feedback for Broadband Matching

C. T. Fu, C. N. Kuo, National Chiao-Tung University, Hsinchu, Taiwan

A 1.5V, 3~11GHz CMOS UWB LNA using dual feedback loops is reported. Using shunt capacitive feedback and series transformer feedback the broadband matching condition is achieved with high flat gain. Fabricated in 0.18um CMOS process, the measurement resul demonstrates power gain of 11dB and maximum NF less than 5.5dB throughout the frequency range from 3- to 11-GHz with power consumption of 10.5mW.

RMO1C-5 9:20 AM

A SiGe Low-Noise Amplifier for 3.1-10.6 GHz Ultra-Wideband Wireless Receivers

B. Shi, Y. W. Chia, Institute for Infocomm Research

This paper presents a SiGe low-noise amplifier for 3.1-10.6 GHz UWB receivers. The LNA uses a circuit topology consisting of two gain stages in multiple feedback loops to achieve broadband flat gain together with low noise figure and good input match. Faricated in a 0.25u SiGe BiCMOS technology, the IC prototype delivers a power gain of 20 dB and a NF of 2.8-4.7 dB over the full UWB band, while achieving an IIP3 of -8 dBm. The amplifier occupies 0.34 mm2 and consumes 11 mA from a 2.7 V supply.

Monday June 12, 2006
8:00 AM
SFCC – Room 304
Session RMO1D: RFIC Technology

Chair: Eli Reese, Triquint Semiconductor
Co-Chair: Admya Gupta, Anadigics

RMO1D-1 8:00 AM

DC/DC Converter Controlled Power Amplifier Module for WCDMA Applications

Jongsoo Lee, Jeff Potts*, Eddie Spears, RF Micro Devices, Phoenix, AZ, *RF Micro Devices, Greensboro, NC

A single package power amplifier module with GaAs PA and Si DC/DC converter for WCDMA application is presented in this paper. Integration of a linear power amplifier and a power management chip is implemented to improve the efficiency of the PA at low ouput power by changing the supply voltage. Overall PA performance at 27.5dBm is identical to the discrete WCDMA power amplifier and the efficiency at 16dBm output power is improved from 8 ~ 9% at 3.4V supply voltage to 16.8% with the converter.

RMO1D-2 8:20 AM

Coupling Effects of Dual SiGe Power Amplifiers for 802.11n MIMO Applications

W.-C. Hua*, P.-T. Lin*, C.-P. Lin*, C.-Y. Lin*, H.-L. Chang*, C. W. Liu*, T.-Y. Yang**, and G.-K. Ma**, *National Taiwan University, Taipei, Taiwan, **Industrial Technology Research Institute, Hsinchu, Taiwan

The coupling effects of dual SiGe PAs on a single chip for 802.11n MIMO applications are demonstrated for the first time. Deep trench isolation and grounded guard ring are used for crosstalk isolation at both transistor and circuit levels. The equivalen small-signal coupling at 2.45 GHz between two PAs is -30 dB. The PA delivers 18.1/16.6 dBm with 3% EVM (OFDM, 64-QAM) in single and dual PA operation modes, respectively. The EVM degradation becomes severe as the interfering power increases.

RMO1D-3 8:40 AM

Integrated Transformer Baluns for RF Low Noise and Power Amplifiers

H. Gan, S. S. Wong, Stanford University

On-chip transformer baluns integrated with an RF front-end architecture for medium power WLAN is presented. Method of characterizing a 3-port balun with a 2-port network analyzer is discussed. Implemented in 0.18μm CMOS, the receive path including a swith, an input transformer and a differential LNA, achieves S21 of 17dB, NF of 4.1dB, and IIP3 of 0dBm at 2.45GHz; the transmit path of a differential PA with an output transformer, achieves Psat of 21dBm, P1dB of 17dBm, and max PAE of 21%.

RMO1D-4 9:00 AM

RF Components with High Reliability and Low Loss by Partial Trench Isolation of SOI-CMOS Technology

A. Furukawa, Y. Hirano*, T. Ohnakado, T. Ikeda*, Y. Kagawa, K. Shintani, K. Nishikawa, S. Yamakawa, T. Ipposhi*, S. Maegawa*, M. Takeda, and H.Arima*, Mitsubishi Electric Corporation, *Renesas Technology Corporation

This paper describes the experimental characteristics of RF components with layout and structural optimization, fabricated in 0.10-um 1.2-V SOI-CMOS technology with partial trench isolation (PTI). Newly- proposed ESD protection diodes and SOI-grounded gae NMOSFET achieve highly reliable performance due to body-tied structure with PTI. Moreover, this technology offers a low loss RF switch and a broadband amplifier with low-power consumption.

RMO1D-5 9:20 AM

Silicon full integrated LNA, Filter and Antenna System Beyond 40 GHz for MMW Wireless Communication Links in Advanced CMOS

S. Montusclat, F. Gianesello, D. Gloria, STMicroelectronics, FTM Crolles R&D, Q-TPS Lab, , 850 rue Jean Monnet, 38926 Crolles Cedex France

Today, SiGe HBT and MOSFET cut-off frequencies are higher than 230 GHz and this increase allows new MMW applications on silicon such as 60 GHz WLAN and 77 GHz automotive radar. This study focuses on a wireless communication block with the antenna integraion. Functions such as amplifier and filter have been used. This is a demonstration of individual component integration and co-integration with antenna/LNA matching in an advanced sub 120nm HCMOS High Resistivity SOI technology at 40 GHz.

Monday June 12, 2006
10:10 AM
SFCC – Room 307-310
Session RMO2A: WLAN & MIMO

Chair: Srenik Meta, Atheros Communications
Co-Chair: Glenn Chang, Maxlinear Inc.

RMO2A-1 10:10 AM Invited

A Fully-Integrated Dual-Band MIMO Transceiver IC

P-B. Leong, S.W. Son, M. Tsai, L. Tse, Marvell Semiconductor

A monolithic MIMO transceiver IC consisting of 2 transmitters and 3 receivers is implemented in a 0.35 um SiGe BiCMOS process. The receivers achieve a NF of 4 dB in 2.4 GHz and 5.5 dB in 5 GHz; while the transmitters deliver an OP1dB of 11 dBm. The MIM transceiver in full operation consumes approximately 260 mA in RX mode and 245 mA in TX mode from a 3V supply.

RMO2A-2 10:30 AM

A Low-power Full-band 802.11abg CMOS Transceiver with On-chip PA

S. C. Yen, Y. Y. Lin, T. M. Chen, Y. M. Chiu, B. I. Chang, K. U. Chan, Y. H. Lin, M. C. Huang, J. Z. Huang, C. H. Lu, W. S. Wang, C. S. Hu, C. C. Lee, Realtek Semiconductor Corp.

A low-power full-band 802.11a/b/g transceiver in 0.15um CMOS technology is presented. It shows 4.4/4dB low noise figures in 2.4/5GHz receiver chains. An on-chip PA delivers 20dBm output P1dB. –40 to 140°C operation temperature is achieved by sensing techique. Concurrent baseband circuit reduces the chip size. And a new IQ compensation scheme is implemented. In addition to high integration and robustness, it consumes 65/75mA (2.4/5GHz) and 200/107mA for RX and TX mode respectively.

RMO2A-3 10:50 AM

An Area-Efficient 5-GHz Multiple Receiver RFIC for MIMO WLAN Applications

L. Khuon, C. G. Sodini, Massachusetts Institute of Technology

This paper presents area-efficient multiple receivers on a single-chip for 5-GHz MIMO wireless LAN systems. Each receiver has an LNA, Q-enhanced image filter, mixer, and LO amplifier but shares a global LO amplifier and distribution circuits for bias andfilter tuning. The receivers are suitable for both spatial diversity and multiplexing. One receiver provides 14 dB gain, consumes 25 mA at 1.8V, and occupies less than 1 sq. mm chip area. The filter has better than 30 dB image rejection.

RMO2A-4 11:10 AM

A Compact High Rejection 2.4 GHz WLAN Front-End Module Enables Multi-Radio Co-existence UP to 2.17 GHz

Chun-Wen Paul Huang, William Vaillancourt, Andrew Parolin, Chris Zelley, and Zeji Gu, SiGe Semiconductor

A 5 x 6 x 1.4 mm 2.4 GHz WLAN front-end module (FEM) capable of supporting multi-radio co-existence up to 2.17 GHz is presented. The FEM features 28 dB gain, 120 mA for 15 dBm output power with EVM < 3% at 54Mbps, < -170 dBm/Hz noise emission up to 2.17GHz, >45 dB receive path rejection up to 2 GHz with insertion loss < 3.5 dB, and >30 dB T/R isolation under 10:1 mismatch at an idle port. All the features provide an easy integration of a WLAN radio into multistandard handsets up to UMTS bands.

RMO2A-5 11:30 AM Invited

MBOA/WiMedia UWB Transceiver Design in 0.13µm CMOS

C.Sandner, S.Derksen, D.Draxelmayr, S.Ek, V.Filimon*, G.Leach**, S.Marsili, D.Matveev, K.Mertens, H.Paule*, M.Punzenberger, C.Reindl, R.Salerno, M.Tiebout*, A.Wiesbauer, I.Winter**, Z.Zhang, Infineon Austria, *Infineon Germany, **Riverbeck UK

A highly integrated, WiMedia/MBOA compliant RF transceiver for Ultra-Wideband (UWB) data communication in the 3-5GHz band is presented. The design includes receiver, transmitter and fast-hopping synthesizer. It is designed in a 0.13um standard CMOS technlogy for a single supply voltage of 1.5V. The receiver features a measured noise figure (NF) of 3.6 to 4.1dB over the three sub-bands. The transmitter supports a maximum TX power of 0dBm at 20dB EVM.

Monday June 12, 2006
10:10 AM
SFCC – Room 305
Session RMO2B: VCOs and Dividers

Chair: Dan Nobbe, Peregrine Semiconductor
Co-Chair: Yann Deval, IXL lab

RMO2B-1 10:10 AM

VCO Phase Noise and Sideband Spurs due to Substrate Noise Generated by On-chip Digital Circuits

M.A. Méndez, J.F. Osorio, D. Mateo, X. Aragonés, J.L. González, Electronic Engineering Department, Universitat Politècnica de Catalunya, Barcelona, Spain

This paper presents the effects of noise generated by realistic digital circuits on RF voltage controlled oscillators (VCO) integrated in the same silicon die. The digital noise is coupled through the common substrate and generates both phase noise and sdeband spurs at the VCO output. The noise coupling and impact mechanisms, and their dependence on the VCO operating conditions (control voltage, gain and bias current) are investigated.

RMO2B-2 10:30 AM

AM-FM Conversion by the Active Devices in MOS LC-VCOs and its Effect on the Optimal Amplitude

B. Soltanian, P. Kinget, Columbia University in the City of New York

Large oscillation amplitudes in diff. MOS LCVCOs modulate capacitances of the switching devices. Thus, the effective tank capacitance and the osc. freq. change w.r.t. the amplitude for a fixed tuning voltage. The freq.-vs-amplitude curve has a maximum fo a diff. amplitude close to the threshold voltage of the MOS devices which corresponds to the optimum amplitude that minimizes AM-FM conversion and phase noise. The analysis is confirmed with simulation and measurement results for a 2GHz VCO.

RMO2B-3 10:50 AM

Fully-Integrated Multi-Standard VCOs with Switched LC Tank and Power Controlled by Body Voltage in 130nm CMOS/SOI

L.Geynet, E. De Foucauld, P. Vincent and G. Jacquemod*, CEA-Leti, 17 rue des martyrs, 38054 Grenoble Cedex 9, France, *LEAT, 250 rue Albert Einstein, 06560 Valbonne, France.

In this paper, the design of two VCOs for wireless multi-standard applications is presented. These circuits have been produced using CMOS/SOI technology, with body voltage to control power consumption and phase noise performance. A new architecture for mlti-standard applications is proposed. To our knowledge, this is the first structure using a balun to change the oscillation frequency and the body biasing to control VCO core current. Four standards are covered: GSM, DCS, Bluetooth, WLAN.

RMO2B-4 11:10 AM

A 5GHz CMOS Low Phase Noise Transformer Power Combining VCO

P. Lai, S. I. Long , University of California at Santa Barbara

A transformer based power combining technique is shown to be an efficient method for reducing VCO phase noise. Higher signal power and resonator Q can be achieved while avoiding breakdown without penalty in tuning range. A CMOS process was used to fabricte the 5GHz VCO. This VCO has a 4dB improvement in phase noise and 2dB improvement in FOM over a simple LC VCO. The phase noise at 1 MHz offset is –125 dBc/Hz. The VCO dissipates 5.5mA with 17.6% tuning range at a 1.5V supply voltage.

RMO2B-5 11:30 AM

A Double-Balanced Injection-Locked Frequency Divider for Tunable Dual-Phase Signal Generation

L. Zhang, H. Wu, Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY

We present an injection-locked divider (ILFD) with a double-balanced structure to generate two signals with tunable phase difference. A circuit prototype was designed and fabricated using a standard 0.18um digital CMOS technology, and generates dual-phas signals at 4.8-6 GHz. The phase difference of the two output signals can be tuned independently by 55 degrees, and differentially by 100 degrees, both centered around quadrature (90 degrees).The phase noise degradation is negligible.

Monday June 12, 2006
10:10 AM
SFCC – Room 306
Session RMO2C: Next Generation LNAs

Chair: Brian Floyd, IBM Research
Co-Chair: Leonard Reynolds, RF Micro Devices

RMO2C-1 10:10 AM

31-34GHz Low Noise Amplifier with On-chip Microstrip Lines and Inter-stage Matching in 90-nm Baseline CMOS

M.A.T. Sanduleanu,G.Zhang*,J.R.Long* , Philips Research Eindhoven,*Electronics Research
Laboratory / Delft University of Technology

A Ka band low-noise amplifier in a 90-nm bulk CMOS technology is presented. The low-noise amplifier comprises two identical cascode stages, with inter-stage matching as gain boosting. The gain boosting circuit improves the gain by 20% and the noise perfrmance by 27% of the cascode LNA. The proposed amplifier achieves a peak power-gain of 19dB with a 3-dB bandwidth of 31 to 34GHz and a noise figure of 3dB in the middle of the band.

RMO2C-2 10:30 AM

60-GHz PA and LNA in 90-nm RF-CMOS

T. Yao, M. Gordon, K. Yau, M.T. Yang*, S.P. Voinigescu, University of Toronto, *TSMC

60-GHz power (PA) and low-noise (LNA) amplifiers implemented in a 90-nm RF-CMOS process with thick 9-metal layer copper backend and transistor fT/fMAX of 140GHz/170GHz are reported. The PA operates from a 1.5V supply and features 5.2dB power gain, 3dB B>13GHz, P1dB of +6.4dBm, saturated Pout of +9.3dBm, and 7% PAE, at 60GHz. The LNA has 14.6dB gain, an input P1dB of -13.6dBm, and a simulated NF of 4.5dB, while drawing 16mA from a 1.5V supply. Both circuits use inductors to minimize area.

RMO2C-3 10:50 AM

A 800-uW 26GHz CMOS Tuned Amplifier

Y. Su, K. K. O, Silicon Microwave Integrated Circuits and Systems Research Group, Dept. of E.C.E, University of Florida

A 26-GHz cascode tuned amplifier with a gain of 8.4dB, NF of ~5dB consuming 800μW from a 1.0-V supply has been demonstrated in 130-nm CMOS technology. To increase the gain at given power consumption, the output resistances of cascode amplifier is increasd by adding a series inductor at the gate of common gate stage. The power consumption of amplifier is more than 5X lower than that of the previously reported CMOS amplifiers operating near 20 GHz.

RMO2C-4 11:10 AM

A 27.7dBm OIP3 SiGe HBT Cascode LNA Using IM3 Cancellation Technique

Sungmin Ock*, Seokyong Hong*, Sangwoo Han*, Joonsuk Lee**, * Future Communications IC Inc., ** McKinsey&Company

1.9GHz low noise amplifier(LNA) is implemented with SiGe BiCMOS process using a modified cascode structure. In order to achieve high linearity and low NF at the same time, the phase of IM3(3rd order inter-modulation) in a common emitter amplifier is deried and the new IM3 cancellation method is proposed. The measurement results of the LNA at 1930MHz are gain of 16.9dB, noise figure of 1.5dB, and OIP3 of 27.7dBm with a single 2.7V supply. It consumes only 4.4mA.

RMO2C-5 11:30 AM

A Wideband Noise-Canceling CMOS LNA Exploiting a Transformer

Stephan C. Blaakmeer, Domine M.W. Leenaerts*, Eric A.M. Klumperink, Bram Nauta, University of Twente, IC-Design Group, The Netherlands, *Philips Research Laboratories, The Netherlands

Low-cost, wideband Low Noise Amplifiers with a bandwidth in excess of 1 GHz are required to implement receivers for future data communication standards. A broadband LNA incorporating single-ended to differential conversion is successfully implemented, usng a noise-canceling technique and a single on-chip transformer. The LNA achieves a high voltage gain of 19dB, a wideband input match (2.5–4.0GHz), and a NF of 4–5.4 dB, while consuming 8mW. The LNA is implemented in a digital 90nm CMOS process.

Monday June 12, 2006
10:10 AM
SFCC – Room 304
Session RMO2D: WLAN Power Amplifiers

Chair: Tina Quach, Freescale Semiconductor
Co-Chair: Noriharu Suematsu, Mitsubishi Electric

RMO2D-1 10:10 AM

A Fully-Integrated +23-dBm CMOS Triple Cascode Linear Power Amplifier with Inner-Parallel Power Control Scheme

H-S. Oh*, C-S. Kim**, H-K. Yu**, and C-K. Kim*, *Korea Advanced Institute of Science and Technology (KAIST), **Electronics and Telecommunications Research Institute (ETRI)

In this paper, we present a triple cascode CMOS linear PA with inner-parallel power control scheme. In the proposed PA, the oxide breakdown problem is substantially relaxed and the efficiency at low power levels is enhanced without linearity degradation nd circuit complexity increase. The fabricated PA fully-integrated in 0.18um CMOS delivers an output power of 23dBm with 35% PAE and 19dB power gain at single-stage. Especially, PAE at 8dB-backoff from 20dBm P1dB is as high as 12%.

RMO2D-2 10:30 AM

A Dynamic Supply CMOS RF Power Amplifier for 2.4GHz and 5.2GHz Frequency Bands

Paulo Augusto Dal Fabbro, Cédric Meinen, Maher Kayal, Kazuhiko Kobayashi* and Yuu Watanabe*, Electronics Laboratory (LEG), EPFL, Lausanne, CH-1015, Switzerland, *Fujitsu Laboratories Ltd., Nakahara-ku, Kawasaki, 211-8588, Japan

An implementation of a dynamic supply RF power amplifier (PA) in 0.11um CMOS technology is presented. Two-tone measurement results at 2.4 and 5.2GHz show that the system can deliver over 16dBm linear output power with efficiencies of 22.7% and 12.6%, resectively. Compared to constant supply operation, besides providing higher linear output power, the dynamic supply technique allows over 230% relative efficiency enhancement at 2.4GHz and 160% at 5.2GHz at low output power levels.

RMO2D-3 10:50 AM

Impedance Optimization of Linearizer to Suppress Intermodulation Distortion in 2.45GHz SiGe WLAN

Power Amplifier, Ji Hoon Kim, Ki Young Kim, Seung Hwan Won, Jae Jin Lee, Yun Hwi Park*, Yul Kyo Jung* , Seok Tae Kim and Chul Soon Park, Information and Communications University,*Samsung Electro-Mechanics Co., Ltd.

An RF power amplifier(PA) for IEEE 802.11g WLAN terminals is implemented with a 33 GHz-fT, 0.8-?-SiGe bipolar technology. This paper demonstrates a linearizer consisting of a varactor and a base-emitter junction diode of a bias transistor. Intermodulatio(IMD) is suppressed by optimized impedance of the linearizer. The reactance is minimized at low output power level for eliminating IMD, and maximized near 1-dB compression point (P1dB).IMD is improved as much as 0.2~6dB up to 20dBm output power.

RMO2D-4 11:10 AM

Fully Integrated Doherty Power Amplifiers for 5 GHz Wireless-LANs

Daekyu Yu, Bumman Kim, Pohang University of Science and Technology (Postech)

Through a new Doherty power amplifier circuit topology, the bulky Doherty in/output matching block including ?/4 impedance transformer can be fully integrated using capacitors, short micro-strip lines and bonding wires. To improve efficiency at a full poer, a new input power driving concept is implemented by using the lumped elements. The amplifier based on InGaP HBT technology, shows a Pout of 22.5 dBm and a PAE of 21.3 % at an EVM of 5 %, measured with 54 Mbps 64-QAM-OFDM signals at 5.2 GHz.

RMO2D-5 11:30 AM

A 5.8GHz, 47% Efficiency, Linear Outphase Power Amplifier with Fully Integrated Power Combiner

A. Pham, C. G. Sodini, Microsystems Technology Laboratory, MIT, Cambridge, MA

This paper presents an outphase power amplifier, consisting of two class-E PAs and a power combiner. Using shielded coplanar striplines, the first low-loss, fully integrated 5.8 GHz Wilkinson combiner is realized with excellent isolation for a robust outhase PA. The outphase PA, fabricated in IBM 7WL SiGe BiCMOS, achieves a peak efficiency of 47% at the maximum output power of 18.5dBm. For an input OFDM signal of 32 sub-channels of 32 sub-channels of 64-QAM, the ACPR is better than 32dBc

Monday June 12, 2006
1:20 PM
SFCC – Room 307-310
Session RMO3A: Cellular ICs II

Chair: Jyoti P. Mondal, Freescale Semiconductor
Co-Chair: Andre Hanke, Infineon

RMO3A-1 1:20 PM Invited

A Single-chip 0.13µm CMOS UMTS W-CDMA Multi-band Transceiver

R. Koller*, T. Ruehlicke**, D. Pimingsdorfer*, B. Adler**, *Danube Integrated Circuit Engineering (DICE) GmbH, A-4040 Linz, Austria, **Infineon Technologies AG, 81677 Munich, Germany

A single-chip, fully-integrated 3G UMTS/W-CDMA transceiver covering all operating bands specified by the current UMTS FDD standard has been implemented in a standard 0.13µm CMOS process for use in FDD mobile applications. The design includes two fractionl-N synthesizers with fully-integrated VCO's, on-chip tuning and PLL's as well as the zero-IF receiver and direct-upconversion transmitter paths.

RMO3A-2 1:40 PM

A Low Voltage (1.8V) Operation Triple Band WCDMA Transceiver IC

H. Tomiyama, C. Nishi, N. Ozawa, Y. Kamikubo, H. Honda, H. Fujita, Y. Kondo, H. Iizuka, T. Takahashi, System LSI Business Group, Semiconductor Business Unit, Sony Corp.

A highly integrated triple band (800MHz/ 1.7GHz/2.1GHz) WCDMA transceiver IC which operates at low voltage (1.8V) is described. All functionalities are implemented in a single chip using a 0.18um SiGe BiCMOS process. The Direct conversion receiver consits of triple band preamplifiers, I/Q demodulators, channel select filters, and PGAs. The Direct transmit upconverter consists of a modulator, a three stage VGA, and triple PA drivers. No TX carrier leakage calibration is needed. Two synthesizers with automatically calibrated VCOs are fabricated on the same chip. The IC draws 35mA in receive and 39-61 mA in transmit using a 1.8v supply voltage.

RMO3A-3 2:00 PM Invited

Fully Integrated CMOS GPS Receiver for System-on-Chip Solutions

C. Grewing, B. Bokinge, W. Einerman, A. Emericks, D. Theil, S. van Waasen, Infineon Technologies Sweden AB, Design Center Stockholm

A CMOS receiver for the GPS is presented. It is designed in a 0.13um CMOS process and is fully integrated for the needs of a SoC for GPS and A-GPS. It provides the needed frequency conversion, gain and filtering for GPS signals without any other externalcomponents than those required for matching and decoupling. The receiver includes the LO signal generation and all needed supply voltage regulator. The achieved NF of the receiver is 1.8dB, including losses of external filters for blocking.

RMO3A-4 2:20 PM

High-Performance Crest Factor Reduction Processor for W-CDMA and OFDM Applications

A. Wegener, Texas Instruments

Highly linear wideband power amplifiers (PAs) are needed for W-CDMA and OFDM modulations. Such PAs have low efficiency because of the high peak-to-average ratio (PAR) of CDMA and OFDM signals. We describe the GC1115 crest factor reduction processor, a .8M gate device fabricated in 130 nm CMOS process. The GC1115 decreases the PAR of W-CDMA Test Model signals to 5.7 dB while meeting all signal quality requirements of 3GPP TS 25.141. The GC1115 achieves similar PAR improvement on OFDM signals

RMO3A-5 2:40 PM Invited

GSM/GPRS Single-Chip in 130nm CMOS: Challenges on RF for SoC Integration

D. Seippel, M. Hammes, A. Hanke, J. Kissing, Infineon Technologies

Since CMOS GSM-radio-transceiver are established on the market a few years ago the next evolutionary step is a complete GSM/GPRS Baseband-RF-SoC integration. It promises lowest production cost, easiest board integration and the highest flexibility in sysem optimization. However, crosstalk from digital into analog and RF blocks is a severe constraint. In this paper we will present the main cross coupling effects and challenges for the RF integration.

Monday June 12, 2006
1:20 PM
SFCC – Room 305
Session RMO3B: PLLs and Synthesizers

Chair: Bertan Bakkaloglu, Arizona State University
Co-Chair: Sunjay Raman, Virginia Tech

RMO3B-1 1:20 PM

A Low-Power FSK Modulator using Fractional-N Synthesizer for Wireless Sensor Network Application,

Dan Lei Yan, T. Hui Teo, Bin Zhao, Yeung Bun Choi, Wooi Gan Yeoh, Institute of Microelectronics, Singapore

A low-power fractional-N synthesizer is designed for direct modulation transmitter at 2.40-2.50GHz range using standard 0.18-µm CMOS. The synthesizer is fully implemented on-chip for integrated low data rate Wireless Sensor Network (WSN) application. Thedata rate is as low as 10kbit/s. Phase noise of -93dBc/Hz at 600kHz offset is measured for the synthesizer. The active area is 0.8?0.8mm2, with total power of 8.0mW from a single 1.8V supply.

RMO3B-2 1:40 PM

A -85dBc Reference Spur Quadratude 1-2.5GHz Dual-path Sampled Loop Filter CMOS PLL with sub-1ºrms Phase Noise

A. Maxim, M. Gheorghe, Crystal Semiconductor Inc.

A wide tuning range multi-GHz frequency synthesizer was realized in a 0.13µm CMOS process using a dual-path sampled loop filter. Both the integral and proportional loop filter paths use sample and hold switched capacitor circuits that completely isolate he oscillator from the charge-pump switching action. A sub-1ºrms integrated phase noise was achieved using a large amplitude crystal oscillator and a low gain ring oscillator. A multi-regulator architecture reduces the supply injected spurs.

RMO3B-3 2:00 PM

A Low Power Bandpass Sigma-Delta Modulator Injection Locked Synthesizer

H.H. Chung, U. Lyles, T. Copani, B. Bakkaloglu, S. Kiaei, Connection One, Arizona State University, Goldwater Center, Tempe, Arizona, 85287

A fully integrated 0.13um CMOS PLL transmitter for on-channel modulation at 2.4GHz ISM band is presented. A bandpass sigma-delta direct digital frequency synthesized reference oscillator is utilized to provide a wideband PLL with a frequency modulated sinal. A single-bit bandpass sigma-delta modulated injection locked oscillator is used as a reference signal. The transmitter achieves a 0dBm output power at 1Mbit/sec when using a 0.5BT GFSK modulation. Measured phase noise is -104dBc/Hz at 1MHz.

RMO3B-4 2:20 PM

A Carrier Frequency Generator for Multi-Band UWB Radios

C. Mishra, A. Valdes-Garcia, E. Sánchez-Sinencio and J. Silva-Martinez, Analog and Mixed Signal Center, Electrical and Computer Engineering Department, Texas A&M University, College Station, TX.

A carrier frequency generator for multi-band UWB radios is presented. It generates 11 carrier frequencies in quadrature in the range of 3.7-10GHz from a single frequency source. The system consists of a series of dividers, single side-band mixers with fitering and multiplexers. The IC is implemented in a 0.25µm SiGe BiCMOS technology and measured in a QFN package. With an active area of 2.2?1.9mm^2 the system draws 75mA of current from a 3V supply.

RMO3B-5 2:40 PM

A Dual Band Quad Mode ?S Frequency Syntheszier

Wei-Zen Chen, and Dai-Yuan Yu , National Chiao-Tung University

This paper describes the design of a dual-band, quad-mode ?-S frequency synthesizer for WLAN a,b,g and Bluetooth application. Integrating both a multi-modulus PLL and a 3rd order ?-S modulator in a single chip, the channel spacing of the RF synthesizer cn be as low as 20 kHz and the frequency hopping time is less than 67 µsec. A new charge pump circuit is proposed to improve its linearity and the matching of the pumping currents. The measured phase noise at 1MHz offset are about -114 dBc/Hz and -116 dBc/Hz respectively at 5 GHz and 2.5 GHz frequency bands. Fabricated in a 0.18-µm CMOS process, the chip size is 1.95 mm2. The total power consumption is 19.54 mW from a 1.8 V power supply .

Monday June 12, 2006
1:20 PM
SFCC – Room 306
Session RMO3C: Silicon-based Millimeter-wave Front Ends

Chair: Georg Boeck, TU Berlin
Co-Chair: Reynold Kagiwada, Northrop Grumman

RMO3C-1 1:20 PM Invited

CMOS Transceivers for the 60-GHz Band

B. Razavi, UCLA

This paper gives an overview of millimeter-wave CMOS transceiver design and presents several critical building blocks operating around 60 GHz. A direct-conversion receiver front end employing new LNA and mixer topologies is presented that exploits resonace by means of folded microstrips to achieve a gain of 27 dB and a noise figure of 12.5 dB while consuming 9 mW. Also, a direct-conversion transmitter incorporting an on-chip dipole antenna is introduced that paves the way for beamforming and MI

RMO3C-2 1:40 PM

A Highly Linear SiGe Double-Balanced Mixer for 77 GHz Automotive Radar Applications

B. Dehlink, H.-D. Wohlmuth**, H.-P. Forstner*, H. Knapp*, S. Trotta, K. Aufinger*, T. F. Meister*, J. Boeck*, A. L. Scholtz, Technical University of Vienna, *Infineon AG, **now with Frequentis GmbH

An active double-balanced mixer for automotive applications in the 77GHz range is presented. The circuit includes on-chip baluns both at the RF and the LO port. The mixer was designed and fabricated in a 200GHz fT SiGe:C bipolar technology. At 77GHz, themeasured conversion gain of the mixer is 11.5dB, and the measured single sideband noise figure is 15.8dB. The input-referred 1dB compression point at 75GHz is -0.3dBm. This mixer is very robust against waver inhomogeneities. Draws 75mA from 5.5V

RMO3C-3 2:00 PM

A 28 GHz Sub-harmonic Mixer Using LO Doubler in 0.18-µm CMOS Technology

Tsung-Yu Yang, and Hwann-Kaeo Chiou, National Central University, Jhongli, Taiwan, R.O.C.

A 28 GHz sub-harmonically pumped passive down conversion mixer fabricated in a 0.18-µm CMOS process is demonstrated. A low power fully differential LO frequency doubler is designed to generate at near half RF frequency. The proposed sub-harmonically pumpd passive mixer has advantages in low power consumption, high fundamental frequency suppression, and suitable apply to millimeter-wave frequencies. At 28 GHz RF frequency and 13.2 GHz LO frequency, the measured conversion loss of the mixer is less than 11 dB, single side band noise figure of 11.6 dB, the isolations among LO, IF and RF are over 33 dB, and a third-order intercept point at the input of 8 dBm, while dissipating total current of 0.6 mA from 1 V supply. To the authors' knowledge, the design achieves the highest figure of merit among published down-conversion mixers operating at similar millimeter-wave frequencies in comparable silicon based technology.

RMO3C-4 2:20 PM

A Compact 35-65 GHz Up-conversion Mixer with Integrated Broadband Transformers in 0.18-µm SiGe BiCMOS Technology

P.-C. Huang, R.-C. Liu, J.-H. Tsai, H.-Y. Chang, H. Wang, J. Yeh†, C.-Y. Lee†, and J. Chern†, Department of Electrical Engineering and Graduate Institute of Communication Engineering,†Taiwan Semiconductor Manufacturing Company

A compact 35-65 GHz Gilbert cell up-convert mixer implemented in 0.18-µm SiGe BiCMOS technology is presented. Integrated broadbandtransformers and meandered thin-film microstrip lines were utilized to achieve chip area of 0.6 mm ? 0.45 mm. The mixer achive a flat conversion loss of 7 ± 1.5 dB and LO suppression of more than 40 dB at the RF port from 35 to 65 GHz. The power consumption is 14 mW from a 4-V supply.

RMO3C-5 2:40 PM

Using Auxiliary Amplifier to Cancel Third-Order Intermodulation Distortion For A 1.9 GHz CMOS Linear Amplifier Design

Kung-Hao Liang, Chien-Chih Ho, Meng-Wei Hsieh and Yi-Jen Chan, Department of Electrical Engineering, National Central University

A new linearization method of microwave amplifier design by canceling the third-order intermodulation component (2f2-f1) is proposed. The main amplifier is combined with an auxiliary amplifier, which is appropriately designed by the gain and bias conditions. The output frequency spectra of the main amplifier are subtracted by this auxiliary amplifier. The third-order distortion will be canceled since these two amplifiers are designed by a differential-pair stage. IIP3 improvement as large as 11 dB has been obtained, where this amplifier achieves a 11.5 dB gain at 1.9 GHz, fabricated by using 0.18 µm CMOS technologies. The circuit consumed 11.5 mA or 11 mA based on the condition of auxiliary amplifier on or off, respectively. The auxiliary amplifier constumes small than 0.8 mW dc power and causes only 0.2 dB gain reduction of the main amplifier.

Monday June 12, 2006
1:20 PM
SFCC – Room 304
Session RMO3D: Passive Components and Matching Advances

Chair: Joseph Staudinger, Freescale Semiconductor
Co-Chair: Francis Rotella, Fujitsu Laboratories of America, Inc.

RMO3D-1 1:20 PM
An Analytical Approach to Parameter Extraction for On-Chip Spiral Inductors With Double-p Equivalent Circuit

J.X. Lu, F.Y. Huang, Y.S. Chi, Southeast University

In this paper, We present a novel analytical approach to parameter extraction based on S-parameter measurement for on-chip spiral inductors with double-p equivalent circuit. The extraction is carried out using a set of characteristic functions derived frm the equivalent circuit without iterative optimization. As verified by a series of inductors fabricated with a 0.18 µm CMOS process, a good agreement between the measured and simulated data over a wide frequency range has been obtained.

RMO3D-2 1:40 PM
High Coupling Transformer in CMOS Technology

Heng-Ming Hsu, Ming-Ming Hsieh, Chien-Wen Tseng, and Kuo-Xun Huang, Department of Electrical Engineering, National Chung-Hsing University, Taichung, 402-27,Taiwan, R.O.C

This study proposes a high coupling transformer using current silicon-based technology. Maintaining identical self inductance of proposed transformer, the different layout configuration is discussed in this work. Moreover, an equivalent circuit is proposd to investigate the device behavior especially for high frequency.

RMO3D-3 2:00 PM
Characterization of Si-Based Monolithic Transformers with Patterned Ground Shield

O. El-Gharniti, E. Kerhervé, J. B. Bégueret, IXL Laboratory at Talence, France

This paper investigates the impact of patterned ground shield on monolithic integrated transformers. The minimum insertion loss is shown to be a useful figure of merit. It is used to evaluate transformer performances. We demonstrate that the use of a paterned ground shield increases the quality factor of both primary and secondary coils. It increases also the mutual coupling coefficient and thus reduces the minimum insertion loss at high frequency, while at low frequency it has no effect.

RMO3D-4 2:20 PM
Design of Coplaner Waveguide On-chip Impedance-Matching Circuit for Wireless Reciever Front-End

R. K. Pokharel, H. Kanaya, F. Koga, Z. Arima, S. Kim, and Y. Yoshida, Department of Electronics, Faculty of Information Science and Electrical Engineering, Kyushu University

Recently, spiral inductors have widely been used instead of resistors in the design of matching circuits to enhance the thermal noise performance of a wireless transceiver. However, such elements usually have low quality factor (Q) and may encounter the elf-resonance in microwave-frequency band which permits its use in higher frequencies, and on the other hand, they occupy the large on-chip space. This paper presents a new design theory for the impedance-matching circuits for a single-chip SiGe BiCMOS receiver front-end for 2.4 GHz-band wireless LAN (IEEE 802.11b). The presented matching circuits are composed of conductor-backed coplanar waveguide (CPW) meanderline resonators and impedance (K) inverter. The prototype front-end receiver is fabricated and measured. A few of the measured results to verify the design theory are presented.

RMO3D-5 2:40
Novel 3 Port Characterisation and De-embedding for High Performance On-Silicon Ka Band Balun

J. A. O'Sullivan, K. G. McCarthy and P. J. Murphy , Department of Electrical and Electronic Engineering, University College Cork, Cork, Ireland

A novel 3 port de-embedding technique is presented. The method is used to accurately characterise the performance of an on-silicon mulitlayer balun. Three de-embedding structures have been fabricated along with the balun itself. From 25 to 40 GHz the de-mbedded balun achieves phase and magnitude imbalances less than 5 degrees and 1 dB respectively. Excellent correspondence between the measured balun parameters and EM simulation results is observed after de-embedding is applied.

Monday June 12, 2006
3:30 PM
SFCC – Room 307-308
Session RMO4A: Wireless Remote Sensing & RFID

Chair: Natalino Camilleri, Alien Technology Corporation
Co-Chair: Steve Lloyd, Beceem Communications Inc.

RMO4A-1 3:30 PM

A Fully Integrated 2.4-GHz CMOS RF Transceiver for IEEE 802.15.4

I-J. Kwon, Y-S. Eo, S-S. Song*, K-D. Choi, H-B. Lee, K-R. Lee*, Samsung Advanced Institute of Technology, Yongin-si, Korea, *KAIST, Daejeon, Korea

A fully integrated 2.4 GHz CMOS transceiver IC for the low power wireless personal area network (WPAN) is reported. This is based on dual-conversion architecture receiver and transmitter, thus suitable for silicon integration. The fully integrated transciver is fabricated in 0.18 um CMOS technology and the die area of the single-chip IC is 3.7 mm x 3.6 mm. It consumes only 31 mW in the receiver mode and 42 mW in the transmitter mode with 1.8-V supply.

RMO4A-2 3:50 PM

An Energy Efficient OOK Transceiver for Wireless Sensor Networks

D. C. Daly, A. P. Chandrakasan, Massachusetts Institute of Technology

A 1 Mbps 916.5 MHz OOK transceiver for wireless sensor networks has been designed in a 0.18-um CMOS process. The RX has an envelope detection based architecture with a highly scalable RF front end. The RX power consumption scales from 0.5 mW to 2.6 mW, wth an associated sensitivity of -37 dBm to -65 dBm at a BER of 10^-3. The TX consumes 3.8 mW to 9.1 mW with output power from -11.4 dBm to -2.2 dBm. The RX achieves a startup time of 2.5 us, allowing for efficient duty cycling.

RMO4A-3 4:10 PM

A 8.0-mW 1-Mbps ASK Transmitter for Wireless Capsule Endoscope Applications

Han Shuguang, Chi Baoyong, Wang Zhihua, Department of Electronic Engineering, Tsinghua University, Beijing, China

A 2.4GHz ASK transmitter suitable for low power wireless capsule endoscope system is presented. The transmitter mainly includes two parts: a 20MHz ASK modulator based on the constant amplitude phase lock loop (PLL) and a direct up-conversion RF circuit. his design, implemented in TSMC 0.25um CMOS process, achieves -23.217dBm output power with the data rate of 1Mbps and dissipates 3.17mA current from 2.5V power supply.

RMO4A-4 4:30 PM

A 2.45-GHz RFID Tag with On-Chip Antenna

W.G. Yeoh, Y.B. Choi, L.H. Guo, A.P. Popov, K.Y. Tham, B. Zhao, X. Chen, Institute of Microelectronics, Singapore.

Powered exclusively by on-chip antenna, a 2.45-GHz RFID tag with RF read/write capabilities has been realized in 0.13-µm CMOS process. By eliminating external antenna, the 0.5-mm2 tag presents a low-cost alternative for achieving high-end features such s bi-directional communication, anti-collision and rewritable memory that are attainable only with off-chip solutions.

RMO4A-5 4:50 PM

Design of Multistage Rectifiers with Low-Cost Impedance Matching for Passive RFID Tags

Ray Barnett, Steve Lazar*, Jin Liu, University of Texas at Dallas, * Texas Instruments

The paper presents analysis of the input impedance, as well as the input capacitance and output resistance of diode doublers and multistage rectifiers. Tradeoffs between device sizes and the number of rectification stages are presented with an emphasis n low cost impedance matching. As a result, it is possible to achieve higher efficiency in RF to DC conversion with low cost impedance matching by using just a strap inductor between the antenna and the rectifier IC. Four diode doublers and three multistage rectifiers have been designed and fabricated using a 0.13um CMOS process with EEPROM. Measurement results are in agreement with the analysis.

Monday June 12, 2006
3:30 PM
SFCC – Room 305
Session RMO4B: UWB Transcever ICs

Chair: Chris Rudell, Intel

Co-Chair: Albert Wang, Illinois Institute of Technology

RMO4B-1 3:30 PM

A 0.18µm CMOS Receiver for 3.1 to 10.6GHz MB-OFDM UWB Communication Systems

Yen-Horng Chen*, Chih-Wei Wang*, Ching-Feng Lee*, Jen-Lung Liu*, Tzu-Yi Yang*, Chih-Fan Liao**, Che-Fu Liang**, Gin-Kou Ma*, Shen-Iuan Liu** , *Industrial Technology Research Institute, **National Taiwan University

A direct conversion receiver for MB-OFDM UWB systems operating in 3.1-10.6GHz is presented. The receive chain provides conversion gain of 77dB with 58dB control range. The NF is about 5.8dB in 3-5GHz, rising to 7.6dB at 8GHz, and still below 9.3dB up to 0GHz. The IIP3 of -10.3dBm and IIP2 of 20.2dBm ensure a linear radio receiver. The circuit is fabricated in 0.18µm CMOS process and mounted on a Rogers4003 PCB for measurement
It consumes 45mA and 38mA for LNA H/L gain mode from 1.8V supply.

RMO4B-2 3:50 PM

A Fully Integrated 3-band OFDM UWB Transceiver in 0.25um SiGe BiCMOS

J. Bergervoet*, H. Kundur*, D.M.W. Leenaerts*, R.C.H. van de Beek*, , R. Roovers*, G. van der Weide*, H. Waite**, S. Aggarwal**, *Philips Research, Eindhoven, the Netherlands, , **Philips Semiconductors, San Jose, CA

A fully integrated transceiver for 3-band OFDM UWB is presented. Implemented in a 0.25um SiGe BiCMOS process, it has a die area less than 4mm2. The dissipation is 47mA, 43mA, and 27mA at 2.7V supply for receiver, transmitter, and synthesizer respectively The chip features DC offset cancellation, a loop-back test mode, a single pin for antenna connection, a 1GHz baseband clock output and is robust against interferers from cellular and ISM bands. Measured EVM is 8%, NF is 4.5dB and iIP3 is -6dBm

RMO4B-3 4:10 PM

A Novel Low Power UWB Transmitter IC

G. D. Lim*, Y. Zheng, W. G. Yeoh, Y. Lian*, Institute of Microelectronics in Singapore, *National University of Singapore in Singapore

In this paper, a novel fully integrated monocycle pulse based UWB transmitter is presented. Fabricated using a 0.18-µm CMOS process, a low-power all-digital UWB pulse generator and modulator is proposed. The modulated pulse is further shaped by a driver mplifier. The transmitted pulses are binary phase modulated and meet the FCC UWB low frequency band (3.1-4.5GHz) spectrum mask specification.

RMO4B-4 4:30 PM

A Schottky Barrier Diode Ultra-Wideband Amplitude Modulation (AM) Detector in Foundry CMOS Technology

Swaminathan Sankaran, K. K. O, SIMICS, Dept. of Electrical and Computer Engineering, University of Florida

Utility of Schottky diodes (SBDs) fabricated in foundry digital 130-nm CMOS tech. is demonstrated by implementing an ultra-wide-band (UWB) amplitude modulation detector consisting of an LNA, a SBD rectifier, and an LPF. The detector is matched to 50 ? frm 0-10.3 GHz and 0-1.7 GHz at the input and output, respectively and almost covers the entire UWB frequency range. The measured peak conversion gain is -2.2 dB, the sensitivity over the band is between -53 and -56 dBm, and DC power is only 8.5mW

RMO4B-5 4:50 PM

An Analog Correlator with Dynamic Bias Control for Pulse Based UWB Receiver in 0.18µm CMOS Technology

S. Dan, S. R. Karri, K. Wong, F. Lin, X. Chen, Institute of Microelectronics, Singapore

This paper presents an analog correlator circuit for pulse-based ultra-wideband (UWB) communication. Dynamic bias control (DBC) is introduced to reduce the contribution from the multiplier offset, integrator leakage and power consumption. Analysis and mesurement of this correlator are presented.

Monday June 12, 2006
3:30 PM
SFCC – Room 306
Session RMO4C: CMOS Front-Ends

Chair: Walid Y. Ali-Ahmad, American University of Beirut
Co-Chair: Frank Henkel, IMST

RMO4C-1 3:30 PM Invited

Fully Integrated Receiver Front-Ends for Cell-Phones in Deep-Submicron CMOS

F. Svelto, Dipartimento di Elettronica, Università degli Studi di Pavia

Leveraging an in-depth analysis of second order inter-modulation distortion in CMOS active mixers, this paper discusses techniques to improve the dynamic range of direct conversion fully integrated RF front-ends. Particular attention is dedicated to low oltage aspects for compatibility with future technology nodes. Integrated circuits solutions, tailored to UMTS and GSM, have been realized and experiments show specifications are met with margin.

RMO4C-2 3:50 PM

A Low-Noise 40-GS/s Continuous-Time Bandpass ?S ADC Centered at 2GHz

T. Chalvatzis, S. P. Voinigescu, The Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto

A 2-GHz, Continuous-Time Bandpass ?S Analog-to-Digital Converter sampled with a 40-GHz clock was implemented in a 130-nm SiGe BiCMOS technology. It achieves an SNDR of 63 dB and 55 dB over 10 MHz and 60 MHz, respectively, and an SFDR of 61 dB with a sinle-ended IIP3 of +4 dBm. The center frequency is tunable between 1.8 GHz and 2 GHz. It employs a Gm-LCVAR filter based on a MOS-HBT cascode transconductor with an NFMIN of 2.3 dB. The ADC consumes 1.6 W from a 2.5-V supply with a figure of merit of 26 pJ/sampled bit.

RMO4C-3 4:10 PM

A Novel IP2 Calibration Method for Low-Voltage Downconversion Mixers

K. Dufrene, R. Weigel, University of Erlangen-Nuremberg, Institute for Electronics Engineering

This paper describes a novel IP2 calibration method for double balanced downconversion mixers. The technique reduces difference between duty cycle mismatches of two switching pairs in the mixer core, being suitable for low-voltage mixers employing common-mode feedback block in the output stage. A tunable IQ mixer prototype, fabricated in a 0.13um RF CMOS technology and operating under low voltage supply of 1.5 V, is presented. Experimental results confirm the feasibility of the tuning approach. the smallest die area, and outputs the highest swing than the ever-reported silicon-based modulator drivers.

RMO4C-4 4:30 PM

A 2.4-GHz Sub-mW CMOS Current-Reused Receiver Front-End for Wireless Sensor Network

T. Song, H.-S. Oh, S. Hong, E. Yoon*, Korea Advanced Institute of Science and Technology (KAIST), *University of Minnesota

A 2.4-GHz fully integrated CMOS receiver front-end using current-reused folded-cascode circuit scheme is presented. A configuration utilizing vertically stacked low-noise amplifier (LNA) and a folded-cascode mixer is proposed to improve both conversion gin and noise figure suitable for sub-mW receiver circuits. The proposed front-end achieves a conversion gain of 31.5 dB and a noise figure of 11.8 dB at 10 MHz with 500 uA bias current from a 1.0 V power supply.

RMO4C-5 4:50 PM

A Transformer Based 1.8 – 1.9GHz Low-IF Receiver for 1V in 0.13µm CMOS

C. Hermann, C. Muenker*, H. Klar, Technical University of Berlin, *Infineon Technologies AG

A fully integrated low-IF receiver for 1.8-1.9GHz has been realized in 0.13-µm CMOS. A design method is presented to reduce the input impedance of the mixer's commutating stage in order to improve the current gain of the on-chip transformer. This helps t improve the IIP3 and to reduce the power consumption. The receiver takes 25.7mA from a 1 V supply to give an IIP3 of -20.3dBm, an 1-dB compression point of -30.7dBm, a conversion gain of 29.2dB and a SSB noise figure of 3.0dB.

Monday June 12, 2006
3:30 PM
SFCC – Room 304
Session RMO4D: Avanced Noise Characterization and Modeling

Chair: Yuhua Cheng , Sliconiinx Inc.
Co-Chair: Louis Liu, Northrop Grumman Corporation

RMO4D-1 3:30 PM

An Analytical Method to Determine MOSFET's High Frequency Noise Parameters from 50 Ohm Noise Figure Measurements

S. Asgaran, M. J. Deen, C-H. Chen, McMaster University, Department of Electrical and Computer Engineering

An analytical method, along with closed-form solutions, for extracting MOSFET's RF noise parameters is presented. This method extracts the minimum noise figure, NFmin, equivalent noise resistance, Rn, and optimum source admittance Yopt, of MOSFET directl from a single high frequency 50-? noise figure measurement. This method can accurately predict the noise parameters of deep-submicron MOSFETs.

RMO4D-2 3:50 PM

Reverse Noise Measurement and Use in Device Characterization

J. Randa, T. McKay*, S. Sweeney**, D.K. Walker, L. Wagner**, D. Greenberg**, J. Tao*, G.A. Rezvani*, National Institute of Standards and Technology, *RF Micro Devices, **IBM

We review the concept of reverse noise measurements in the context of on-wafer transistor noise characterization. Several different applications of reverse noise measurements are suggested and demonstrated. Reverse measurements can be used to check measuement results, to significantly reduce the uncertainty in |?opt|, to reduce the occurrence of unphysical results, and possibly to directly measure or constrain parameters in models of transistors.

RMO4D-3 4:10 PM

65-nm 160-GHz RF n-MOSFET Intrinsic Noise Extraction and Modeling using Lossy Substrate De-embedding Method

J. C. Guo, Y. M. Lin, Department of Electronics Engineering, National Chiao-Tung University

A lossy substrate model for accurate simulation of extrinsic noise and a lossy substrate de-embedding method for precise extraction of intrinsic noise have been proven by 80 nm, super-100 GHz fT RF nMOS. The method is further applied to 65 nm 160-GHz fT MOS to investigate aggressive gate length scaling effect on RF noise. The extrinsic noise reveals abnormally weak dependence on gate length scaling even with 50~60% improvement on fT but strong dependence on finger number. The intrinsic noise extracted through lossy substrate de-embedding can consistently reflect the gain in fT and weak dependence on finger number. The NF min at 10 GHz can be suppressed to 0.5dB for 65 nm nMOS corresponding to an optimized drain current, which is around 0.2 dB improvemente.

RMO4D-4 4:30 PM

A 0.18 um Dual-Gate CMOS Model for the Design of 2.4 GHz Low Noise Amplifier

Kung-Hao Liang, and Yi-Jen Chan , Department of Electrical Engineering, National Central University, Taiwan R.O.C.

A dual-gate TSMC 0.18 um gate-length n-MOS has been measured and characterized. The modified dual-gate large-signal model consists of two intrinsic, single-gate conventional BSIM3v3 nonlinear models and the passive network is proposed representing the deice parasitic effects. Good agreement has been obtained between the simulation results of the equivalent circuit model and the measured data up to 15 GHz. A 2.4 GHz dual-gate low noise amplifier was designed based on this modified model.

RMO4D-5 4:50 PM

Power Supply Rejection for Common-Source Linear RF Amplifiers: Theory and Measurements

J. T. Stauth and S. R. Sanders, Department of Electrical Engineering and Computer Science, University of California, Berkeley

This paper describes estimation of the distortion products that arise from power supply noise mixing with the RF signal in a common-source amplifier configuration. Classical Volterra-series system analysis is extended to use on a multiple-input system ad the second order supply ripple sidebands are predicted relative to the magnitudes of the input signal and supply ripple. The analysis is shown to be in good agreement with BSIM3v3 simulation and lab measurements in 180nm CMOS.

Tuesday June 13, 2006
8:00 AM
SFCC – Room 302
Session RTU1A: Wideband Communication System & ICs

Chair: Ranjit Gharpurey, UT Austin
Co-Chair: Madhukar Reddy, Maxlinear Inc.

RTU1A-1 8:00 AM Invited

A CMOS Quadrature Down-Conversion Mixer with Analog I/Q Correction Obtaining 55db of Image Rejection for TV on Mobile Applications

Marc Notten. Maxime Bernard**, Vincent Rambeau, Jan van Sinderen**, * Philips Research Laboratories Eindhoven, The Netherlands, ** Philips Semiconductors Caen, France

An analog I/Q correction system has been developed to lower the power consumption of a quadrature mixer in a silicon TV-tuner intended for mobile applications. The image rejection of this mixer is limited to about 40 dB and the target is 57 dB. The passie CMOS quadrature mixer with I/Q correction is realized, achieving the matching properties of a double quadrature mixer and obtaining more than 55 dB of image rejection and a high dynamic range over a wide frequency range consuming 27mW at 2.7V.

RTU1A-2 8:20 AM

Distributed Amplifiers with Non-Uniform Filtering Structures

Yunliang Zhu and Hui Wu, Department of Electrical and Computer Engineering, University of Rochester

This paper presents a new design concept to control both passband and stop-band characteristics of distributed amplifiers (DAs) by using non-uniform filtering instead of constant-k sections. Two circuit prototypes with Butterworth and Chebyshev filteringwere designed using network synthesis method, and implemented in a 0.18um CMOS technology. The Butterworth one achieved 11.7dB gain, 9GHz bandwidth, and -5dB/GHz roll-off. The Chebyshev one achieved 10dB gain, 8.5GHz, and -8dB/GHz roll-off.

RTU1A-3 8:40 AM

A Fully Integrated 24 GHz SiGe Receiver Chip in a Low-cost Micro-lead Plastic Package

I. Gresham, A. Jenkins, N. Kinayman, R. Point, A. Street, Y. Lu, A. Khalil, R. Ito, R. Anderson, M/A-COM, Lowell, MA 01853

A fully integrated, plastic packaged, 24 GHz SiGe receiver chip is presented. It can be used in a variety of applications including automotive radar sensors and phased-array receivers. The receiver supports two channels which can be used to support sum nd delta antenna pattern inputs commonly employed in automotive radar systems. The receiver comprises of two LNAs, a DPST switch, an I/Q downconverter, babaseband variable gain amplifiers, and integrate-and-dump filters.

RTU1A-4 9:00 AM

A Fully-Integrated 0.13µm CMOS Low-IF DBS Satellite Tuner Using a Ring Oscillator Based Frequency Synthesizer

A. Maxim, R. Poorfard, R. Johnson, P. Crawley, J. Kao, Z. Dong, M. Chennam, T. Nutt, D. Trager, Silicon Laboratories Inc.

The first low-IF fully-integrated tuner for DBS satellite TV applications was realized in 0.13µm CMOS. A wideband ring oscillator based frequency synthesizer having a large frequency step was used to down-convert a cluster of channels to a coarsely defind low-IF frequency, while the second down-conversion to baseband was performed in the digital domain. Eliminating the oscillator inductors allowed a single-chip tuner-demodulator integration, while bringing a significant die area reduction.

RTU1A-5 9:20 AM Invited

Millimeter-Wave Wireless Personal Area Network Systems

Hiroyo Ogawa, National Institute of Informaion and Communications Technology (NICT)

A Millimeter-wave Wireless Personal Network (WPAN) system is designed to provide short-range, high-speed multi-media data services to terminals in rooms or office space. Millimeter-wave ad-hoc wireless access system has been developed by the Yokosuka Reearch Park (YRP) collaborated group which was organized by NICT Yokosuka Radio Communication Research Center. This system is designed to provide easy connectivity, network flexibility and high transmission data rate suitable for WAPN service.

Tuesday June 13, 2006
8:00 AM
SFCC – Room 304
Session RTU1B: Advanced ICs for Optical Communications

Chair: Stefan Heinen, RWTH Aachen University
Co-Chair: Jenshan Lin, University of Florida

RTU1B-1 8:00 AM

A 9.953-12.5GHz 0.13µm Standard CMOS Bondwire LC Oscillator Using a Resistor-Tuned Varactor and a Low-Noise Dual-Regulator

A. Maxim, C. Turinici, Integrated Products, Austin TX

A multi-standard LC oscillator for 10Gb/s SERDES applications was realized in a 0.13µm digital CMOS process. The phase noise was reduced by using a high resolution calibration network that reduces the oscillator gain below 100MHz/V. A low process variatin varactor was realized with constant metal capacitors and voltage controlled resistors. The AM-to-PM conversion was reduced with a supply pushing cancellation circuit. A dual regulator was used to ensure the low noise and high PSRR VCO supply.

RTU1B-2 8:20 AM

10 GHz VCO for a 0.13um CMOS Sonet CDR

W. S. Titus, J. G. Kenney, Analog Devices

A 10 GHz VCO with 1.3:1 KVCO variation and 2 MHz/V supply pushing is developed for a dual channel Sonet CDR IC using MOS inversion mode varactors with their backgates tied to a common mode voltage and with an automatic leveling loop to control oscillatoramplitude and varactor linearization. Three such oscillators are combined with buffers and a passive switch MUX to achieve an 8-12 GHz tuning range and 27mW DC power consumption on a 1.8V unregulated supply. The VCOs are fabricated in a 0.13um CMOS digital process with added MIMCAP support but thin metal interconnect using thick oxide transistors normally provided for 3V I/O. A moderate -112 dBc/Hz phase noise at 1 MHz offset is achieved which is sufficient to exceed OC-192 Sonet random jitter generation.

RTU1B-3 8:40 AM

A 40-Gb/s, Digitally Programmable Peaking, Limiting Amplifier with 20-dB Differential Gain in 90nm CMOS,

J. Weiss, M. L. Schmatz, H. Jäckel*, IBM Zürich Research Laboratory, *Swiss Federal Institute of Technology, ETH Zurich

A 40-Gb/s differential CMOS limiting amplifier in standard 90-nm technology is presented. The circuit dissipates as little as 80 mW from a 1 V power supply and has a differential gain of 20 dB. It can drive data at 40 Gb/s into multiple sampling latches ith a total input capacitance of up to 300 fF. The amplifier features a digitally programmable load resistor for the differential stages to control gain-peaking intensity. Among others, this can be used for cancelling process variations.

RTU1B-4 9:00 AM

Transmitter and Receiver Circuits for Serial Data Transmission over Lossy Copper Channels for 10 Gb/s in 0.13um CMOS

F. Weiss, D. Kehrer, A. L. Scholtz*, Infineon AG, *Technical University of Viena

This paper presents a transmitter and receiver for high speed serial data links including pre-distortion and equalization circuits. The circuits allow data transmission over lossy copper channels up to 10 Gb/s and beyond. The transmitter uses a three tapFIR-filter for pre-distortion. A full rate FIR design allows a low latency and provides a smooth filter characteristic. An analog equalizer in the receiver with high-pass filter characteristic is implemented...

RTU1B-5 9:20 AM

An SOI CMOS, High Gain and Low Noise Transimpedance-Limiting Amplifier for 10Gb/s Applications

F. Pera *, S.P. Voinigescu **, * insyte(Innovative System and Technologies Corp.), ** University of Toronto

This paper presents a low noise, high gain transimpedance-limiting amplifier (TIALA) design for 10Gb/s applications, implemented in a 0.13um SOI CMOS technology. Powered from a single 1.5V supply and consuming 165mW, the TIALA features auto-zero DC feedbck and has 25uApp input current sensitivity (an estimated -16 dBm optical sensitivity) with over 40 dB electrical dynamic range and 14 kOhm linear gain.

Tuesday June 13, 2006
8:00 AM
SFCC – Room 305
Session RTU1C: RFIC Simulation and Layout Optimization

Chair: Kevin McCarthy , University College Cork
Co-Chair: Louis Liu, Northrop Grumman Corporation

RTU1C-1 8:00 AM Invited

Verification of RF Transceivers in SOC: RF, IF, Baseband and Software

K. Muhammad, B. Staszewski, T. Murphy, I. Elahi, Texas Instruments Inc., Dallas, Texas

Single-chip RF SoCs are seeing widespread acceptance in wireless applications. In this paper we address the issue of design verification of such complex ICs that accept input close to the RF carrier frequency and are analyzed for receiver BER performance and transmitter output distortion and phase noise by processing several thousand packets of baseband information while compensation algorithms are simultaneously executed. No comprehensive methodology exists to date for designing such complex systems. This paper present a novel approach that allows building complex RF SoC systems based on VHDL modeling and simulation and opens up major avenues of model development for RF and analog circuits. This approach has been successfully applied to verify two generations of digital RF processors in deep-submicron technologies.

RTU1C-2 8:20 AM Invited

Next-Generation Silicon Analysis Tools for RF Integrated Circuits

A. Mehrotra, A. Narayan, R. Subramanian, Berkeley Design Automation, Inc.

This paper introduces a powerful new generation of analog IC analysis technology designed to address the verification challenges in the design of RF ICs. We summarize what types of problems characterize the design of these circuits and render the verifiction problem difficult. We introduce a new silicon analysis engine based on innovations in mathematics applied to electronic circuit analysis. We present results using this engine on commercial circuits (PLLs, ADCs, transceivers) vs silicon.

RTU1C-3 8:40 AM

A Unified Modeling and Design Methodology for RFICs Using Parameterized Sub-Circuit Cells

D. H. Shin, C. P. Yue, Carnegie Mellon University

This paper presents, for the first time, a cell-based modeling and design platform for RFICs aiming to shorten design cycle time by eliminating iterations between schematic and post-layout simulations and to minimize the risk for costly mask re-spin. By exploiting the modularity in RF circuits at the sub-circuit level, the proposed design platform achieves a balance between circuit design flexibility and device model accuracy compared to the conventional approach.

RTU1C-4 9:00 AM

Layout Optimization of RF CMOS in the 90nm Generation, A. Nakamura, Member IEEE

N. Yoshikawa*, T. Miyazako*,, T. Oishi, H. Ammo, K. Takeshita, Modeling Development Section, Analog &RF Device Development Department, Semiconductor Technology Development Group, Semiconductor Business Unit,*System LSI Business Gp

The multi-finger layout optimization of RF CMOS in the 90nm generation based on a physics-based model is presented. The key features of the physics-based model are that 1) the model includes a wiring and substrate model of the multi-finger layout, and 2)the physical parameters are adopted from DC measurements and TCAD simulation. The dependence of ft /fmax on Wfis simulated within 12% accuracy. After optimization, fmax experiment data showed a 40% increase (166GHz) from the initial layout.

RTU1C-5 9:20 AM

Circuit Model of a SiGe HBT Flip-Chip Mounted onto a Silicon Carrier

M. Norling, and S. Gevorgian, Department of Microtechnology and Nanoscience MC2, Chalmers University of Technology, Gothenburg, SE-41296, Sweden

This paper reports the circuit model of a SiGe HBT transistor flip chipped onto a high resistivity silicon carrier (substrate). It includes the parasitic capacitances and inductances associated with bumps, the flipped transistor chip and takes into accout the effect of the high-permittivity ferroelectric film deposited on the silicon carrier

Tuesday June 13, 2006
8:00 AM
SFCC – Room 306
Session RTU1D: Cellular Bands Power Amplifiers

Chair: Freek van Straten, Philips Semiconductors
Co-Chair: David Ngo, RFMD

RTU1D-1 8:00 AM Invited

Average Current Reduction in (W)CDMA Power Amplifiers

D. A. Teeter, E. T. Spears, H. D. Bui, H. Jiang, D. Widay, RF Micro Devices

Abstract (Invited) — Statistical average current consumption of conventional CDMA and WCDMA [(W)CDMA] power amplifiers is compared to that obtained by using DCDC converters, analog bias control, and low power efficiency enhancement (LPEE) techniques. Adiscussion of theoretical limits, strengths, and weaknesses for each approach is presented.

RTU1D-2 8:20 AM

A 2.4-V Low-Reference-Voltage Operation, InGaP HBT MMIC Power Amplifier Module for CDMA Applications

T. Moriwaki, K. Yamamoto, H. Otsuka*, S. Suzuki, N. Ogawa, K. Maemura, and T. Shimura, Mitsubishi Electric Corporation, *Wave Technology, Inc.

This paper describes circuit design and measurement results of a newly developed InGaP/GaAs HBT MMIC power amplifier module (PA) which can operate with 2.4-V low reference (Vref) and supply voltages of its on-chip bias circuits. New circuit design techniues incorporated into the IC to achieve a 2.4-V low Vref operation allows the PA to deliver a Pout of 27.5-28dBm, a PAE of 39-42% at a Vcc of 3.5 V over a -10 to 90 deg/C wide temperature range while satisfying J- and W-CDMA ACPR specifications.

RTU1D-3 8:40 AM

Large-Signal Characterization of an 870MHz Inverse Class-F Cross-Coupled Push-Pull PA using Active Mixed-Mode Load-Pull

M.P. van der Heijden, D.M.H. Hartskeerl, I. Volokhine, V. Teppati*, A. Ferrero*, Philips Research Laboratories, *Politecnico di Torino

An inverse class-F cross-coupled push-pull PA in a 0.5um SiGe technology is presented. It is shown that inverse class-F in combination with CBC compensation is preferred over class-F operation in terms of gain roll-off and efficiency as function of colletor supply voltage. The active mixed-mode load-pull system is used to set up the proper output differential and common-mode impedances at the fundamental (870MHz) and harmonics to experimentally verify inverse class F operation.

RTU1D-4 9:00 AM

A Fully-Integrated 900-MHz CMOS Power Amplifier for Mobile RFID Reader Applications

J. Han, Y. Kim, C. Park, D. Lee, and S. Hong, Dept. of EE, KAIST, Daejeon, 305-701, Korea

A 900-MHz linear PA for UHF RFID reader was fabricated in a 0.25-um CMOS technology. An on-chip transmission-line transformer is used for output matching network. Input/inter-stage matching components and RF choke inductors are also integrated in the ciruit so that no additional components are required. The power amplifier provides linear output power of 27 dBm at 920 MHz with a 2.5-V supply. PAE at P1dB is 28 %. Gain flatness over the full UHF RFID band, which is from 860 to 960 MHz, is 1 dB.

RTU1D-5 9:20 AM

A CMOS Power Amplifier for Full-Band UWB Transmitters

C. Lu, A. Pham, M. Shaw*, University of California at Davis, *Tahoe RF Semiconductor Inc.

The first CMOS power amplifier that masks exactly over the full-band of ultra wide-band applications is presented. The amplifier also features flat gain and out-of-band suppression. The amplifier achieves a gain of 10.46dB, and the return loss is less thn -10dB. The output P1dB is above 5.6dBm, and OIP3 is higher than 16.6dBm from 3GHz to 10GHz. The group delay dispersion is near zero, and the time domain measurements demonstrate a faithful signal reproduction for wideband large signals.

Tuesday June 13, 2006
1:30 PM
SFCC – Room 103-104
Session RTUIFR: Interactive Forum

Chair: Jenshan Lin, University of Florida
Co-Chair: Luciano Boglione, IECI

RTUIFR-01 1:30 PM

A 2.4GHz Direct Conversion Transmitter for Wimax Applications

C. Masse, Analog Devices, Inc., Wilmington MA, USA

The evolving 802.16 standards offer the possibility of high data rate wireless access for home and business users. The use of OFDM modulation translates into challenging requirements for the transmitter, and more specifically low distortion, good signalbalance and low phase error. This article focuses on the challenges and advantages associated with implementing a direct conversion transmitter for Wimax of 2.35 GHz. The complete signal chain is described along with measured performance.

RTUIFR-02 1:30 PM

A 2.4GHz CMOS RF front-end for Wireless Sensor Network Applications

M. Annamalai,K.F.Ong,Y.B.Choi,W.G.Yeoh, Institute of Microelectronics, Singapore

A 2.4-GHz fully-differential RF front-end on 0.18-µm CMOS technology for wireless sensor network (WSN) applications consuming 4.8-mW from a 1.8-V supply is presented. The direct conversion RF-front end comprises of low-noise amplifier (LNA), I/Q Direct-cnversion mixers, quadrature LO generator and LO buffers. By employing conventional source degenerated LNA, passive mixer, to eliminate flicker noise, RC poly-phase filter for quadrature LO generation, and LO buffers with current reuse technique, we achieve 23-dB conversion gain, 8.1-dB Noise figure, -15- dBm IIP3 and better than 15-dB input return loss for the RF front-end.

RTUIFR-03 1:30 PM

1-11 GHz Ultra-Wideband Resistive Ring Mixer in 0.18-µm CMOS Technology

Tienyu Chang, Jenshan Lin, University of Florida

In this paper, an ultra-wideband downconversion resistive ring mixer is designed using the mixedmode TSMC CMOS 0.18-µm technology. This mixer downconverts RF signals in the range of 1-11 GHz to fixed IF of 500MHz using LO signals at 500MHz higher than the corresponding RF frequencies. The conversion loss within this band is 7±0.5dB. The input 1dB compression point (P1dB) for the entire band is about 5dBm, and the input third order interception point (IIP3) is about 10dBm. The LO power required to obtain lowest conversion loss for this resistive mixer is 9dBm. The mixer core has no power consumption whereas the IF output buffer consumes 3mW. This mixer can be used in high dynamic range low-power ultra-wideband communication systems.

RTUIFR-04 1:30 PM

Receiver RF Front-End with 5GHz-Band LC Voltage-Controlled Oscillator and Subharmonically-Locked Oscillator for 17GHz Aplications

Aleksandar Tasic, Stephen S.Y. Yue*, Dennis K.L. Ma**, Wouter A. Serdijn, John R. Long and David L. Harame***, Delft University of Technology, The Netherlands, *ATI Technologies, Canada, **Synopsys, Canada, ***IBM Microelectronics, Burlington, USA

A 17GHz RF receiver front-end consisting of an LNA, dual balanced mixers, an LC VCO, and a frequency tripler implemented using a ring oscillator is presented in this paper. For a 1.3-3V range in VCO tuning voltage, the locking range of the tripler is 5.5Hz (16.1GHz-21.6GHz). The receiver front-end conversion gain is 13.2dB with a noise figure of 7.1dB and a 3rd-order input intercept point of –6.2dBm. The 1.84mm2 testchip draws 36mA from a 2.2V supply.

RTUIFR-05 1:30 PM

A Transformer-Based Receiver Front-End for 5-GHz WLANs

E. Ragonese, A. Italia, M. F. Seminara*, and G. Palmisano, Università di Catania, Facoltà di Ingegneria, DIEES, ITALY, *STMicroelectronics, Catania, ITALY

In this paper a transformer-based receiver front-end for 5-GHz wireless local area networks is presented. The circuit is implemented in a low-cost 46-GHz-fT silicon bipolar process and includes a variable-gain low noise amplifier and a double-balanced mixer. The front-end does not require any external input balun for the single-ended-to-differential conversion of the RF signal, which is provided by the transformer load of the low noise amplifier.
The receiver front-end exhibits a 4.3-dB noise figure and a power gain of 21 dB. By adopting a 1-bit gain control, the circuit achieves an input 1-dB compression point of -11 dBm, while drawing only 22 mA from a 3-V supply voltage. Finally, thanks to integrated notch LC filters, the front-end provides an on-chip image rejection ratio as high as 50 dB, thus reducing the required selectivity and hence the cost of the external RF filter.

RTUIFR-06 1:30 PM

A Miniature 15-50-GHz Medium Power Amplifier

Mei-Chen Chuang, Pei-Si Wu, Ming-Fong Lei, Huei Wang, Yu-Chi Wang*, and Chan Shin Wu*, Dept. of Electrical Engineering and Graduate Institute of Communication Engineering,National Taiwan University, Taipei, Taiwan, 106, ROC, *WIN Semiconductors Corp.

A miniature power amplifier, which combines two conventional distributed amplifiers and a single transistor amplifier is designed to achieve wide bandwidth, high gain and moderate output power from 15 to 50 GHz. This circuit was fabricated using 0.15-µm aAs based pHEMT MMIC technology. The measured small signal gain is 21±1.5dB from 15 to 50 GHz, and the output saturated power is 18-22 dBm from 18 to 50 GHz with a miniature size of 1.5 x 1 mm2.

RTUIFR-07 1:30 PM

Linear RF Polar Modulated SiGe Class E and F Power Amplifiers

J. D. Kitchen, I. Deligoz, S. Kiaei, B. Bakkaloglu, Arizona State University

Two fully-integrated linearized polar modulated class E and F power amplifiers (PA) with switch-mode supply modulation are presented. The PAs are implemented in a .18um SiGe BiCMOS process and can be used to transmit varying envelope RF signals operatingat 870-920MHz with envelope bandwidths up to 1.3MHz and 16dB dynamic range. Using delta modulation to digitally control the supply, the class E and F PAs have efficiencies of 47% and 45% respectively with output powers of 25.2dBm and 19.1dBm.

RTUIFR-08 1:30 PM

LDMOST Integrated Doherty Amplifier

I.Blednov,J v d Zanden, Philips Semiconductors, The Netherlands

To our knowledge a first high power integrated Doherty amplifier in SOT502 package has been developed for WCDMA applications. This solution is based on 10W MMIC Doherty cell paralleled to achive an output power as high as 120W. The MMIC isbased on the latest Philips LDMOS technology (Gen 6) and showed state of the art performance. 42% Eff has been measured at IMD3 level of –40dBc. We believe this option will lead to a lower cost, more reliable and manufacturable Doherty product.

RTUIFR-09 1:30 PM

SiGe Integrated mm-Wave Push-Push VCOs with Reduced Power Consumption

R. Wanner, R. Lachner*, G.R. Olbrich, Technische Universität Muenchen, Germany, Infineon Technologies, Germany

We have designed and fabricated several push-push VCOs within the frequency range 67 to 75 GHz. In this paper we present one of these oscillators which can be tuned from 71.3 GHz to 75.8 GHz. In this tuning range the measured output power is 3.5 +- 0.4 Bm with an DC to RF efficiency eta = 1.6%. The measured single sideband phase noise is below -105 dBc/Hz at 1 MHz offset frequency. With a reduced supply voltage the efficiency can be increased to eta = 3.5% with an RF output power of 1.5 dBm.

RTUIFR-10 1:30 PM

A Wide Operation Range CMOS Frequency Divider for 60GHz Dual-Conversion Receiver

Y.-J. E. Chen, S.-Y. Bai, T.-N. Luo, and D. Heo*, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan., *School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA 99164 , USA.

This paper presents a wide operation range 0.18um CMOS frequency divider for 60GHz wireless applications. The direct injection lock technique is used to perform the signal division. The deep n-well is implemented under the NMOS switch transistor to improe the lock range of the frequency divider. Combined with band switching and analog frequency tuning, the operation range of the frequency divider covers from 43 to 49 GHz. Operated at 1V, the frequency divider consumes 8mW.

RTUIFR-11 1:30 PM

A 18-GHz Silicon Bipolar VCO with Transformer-Based Resonator

A. Scuderi, E. Ragonese, T. Biondi*, and G. Palmisano, Università di Catania, Facoltà di Ingegneria, DIEES, ITALY, *STMicroelectronics, Catania, ITALY

A silicon bipolar voltage-controlled oscillator for 17-GHz ISM band is presented. The VCO is composed of a core oscillating at 9 GHz followed by a frequency doubler. It adopts a transformer-based topology to obtain both wide tuning range and low noise pefor-mance. The VCO exhibits a tuning range of 4.1 GHz from 16.4 to 20.5 GHz and a phase noise as low as -109 dBc/Hz at a 1-MHz fre-quency offset from a carrier of 18.5 GHz. To design and optimize the resonator, a lumped scalable model for differential driven inductors and transformers was used. This model is presented and validated up to 20 GHz by comparison with experimental data. Index Terms – Integrated transformer, patterned ground shield, sil-icon technology, voltage-controlled oscillator.

RTUIFR-12 1:30 PM

A Sub-mA FH Frequency Synthesizer Technique

E. Lopelli, J. van der Tang*, A. van Roermund, Eindhoven University of Technology, *ItoM

A novel frequency-hopping spread-spectrum transmitter architec-ture is presented that provides robust communications in the 915 MHz ISM band. A base-band predistortion algorithm allows hop-ping with minimum hardware complexity. A 1kbps, 1khop/s link with aBER smaller than 1.1% has been achieved at -25 dBm output power while having 64 orthogonal channels. The synthesizer archi-tecture dissipates only 870 uA, a factor eight less than the state-of-the-art hopping synthesizers.

RTUIFR-13 1:30 PM

14-mW 5-GHz Frequency Synthesizer With CMO Logic Divider and Phase-switching Dual-Modulus Prescaler

Myeungsu.Kim, T.J.Park, Youngil.Kwon, JoonHyung.Lim, S.G. Park, *S.H.Kim, IC Design center of Central R&D, Samsung Electro-Mechanics, *EMD Lab of Central R&D, Samsung Electro-Mechanics

A 5-GHz frequency synthesizer for ZIGBEE(IEEE 802.15.4) is implemented. It consumes only 14-mW adopting CMOS Logic divider and phase-switching dual-modulus.The phase switching is made between the 45° spaced output phases to further reduce the power consuption and improve the robustness of circuit. it con-sumes 8mA at 1.8V and offers 100kHz-loop bandwidth and -103dBc/Hz at a offset of 1MHz. the lock time is 30us. the tuning range is 9.25%,from 2.37GHz to 2.6GHz

RTUIFR-14 1:30 PM

A 1 GHz Sigma-Delta Noise Shaper for All Digital PLLs with Multiband UMTS Modulation Capability,

Thomas Mayer, Volker Neubauer*, Ulrich Vollenbruch**, Tindaro Pittorino, Linus Maurer*, Andreas Springer, Johannes Kepler University Linz, *DICE GmbH & Co KG, **Linz Center of Mechatronics

Fully digital phase locked loops for wideband phase modulation set tough requirements on the digitally controlled oscillator. To get a small frequency step size as well as a large tuning range, oversam-pling at the DCO can be applied. This paper describe the detailed requirements of a 1 GHz oversampling circuit for UMTS modula-tion. A noise shaper enabling the realization of a UMTS compliant DCO design is proposed. The implementation of an 8 Bit Sigma-Delta-Modulator in 0.13um CMOS is shown.

RTUIFR-15 1:30 PM

Tailoring On-Chip Inductors For Low-Noise Ultra-Wide-Band Receiver Applications

Francis K. Chai, Ivan To, Donna Hammock and Margaret Huang, Microwave & Mixed-Signal Technologies Laboratories, Freescale Semiconductor Inc.

Silicon on-chip inductors are effective in UWB receiver applications for simultaneously achieving noise and impedance matching. However, the conventional approach of optimizing on-chip induc-tor quality Q factor for low-GHz narrow-band applications is notap-propriate for wideband UWB receiver front-end designs. This is especially severe for applications approaching 10GHz. Suitable inductor dimensions as well as the inductance values need to be carefully chosen to ensure minimized noise.

RTUIFR-16 1:30 PM

High Performance NPN BJTs in Standard CMOS Process for GSM Transceiver and DVB-H Tuner

Jedon Kim, Hansu Oh, Chulho Chung, Joo-Hyun jeong, Hyunwoo Lee, Seok-Hee Hwang,, In-Chul Hwang, Young-Jin Kim, Kyushik Hong, Eunseung Jung, Kwang-Pyuk Suh, System LSI Business, Samsung Electronics Co., Ltd.

We report a high performance NPN BJT processed in CMOS process that is applied to RFICs. Optimized NPN BJT has current gain of ~44, collector-emitter breakdown voltage of ~7V, collector-base breakdown voltage of ~20V, Early voltage of ~25V, fT of ~8.0GHz and fMAX of ~11.6GHz. The low 1/f noise of BJT resulted in a cor-ner frequency of ~2kHz, which is ~ 4 orders lower than that of NMOS at same current level. The low noise NPN BJT is used to real-ize the ZIF DCR for GSM transceiver and DVB-H tuner.

RTUIFR-17 1:30 PM

Why Reciprocal Procedure Works?

T.Jamneala, D.A.Feld, D.Blackham*, K.H.Wong*, B.Zaini, Avago Technologies,Inc., *Agilent Technologies,Inc.

Accurate characterization of the Short-Open-Load-Thru (SOLT) calibration standards is crucial if correct measurements are to be obtained. For most reciprocal devices (with S12=S21) if the calibration coefficients are inaccurate, the calibrated S21A and S2A values appear not to be identical over all frequencies. We find that we can use this apparent violation of reciprocity to develop a novel procedure for standard characterization. This procedure (''reciprocal procedure'') searches for the optimum set of calibration coefficients for which the reciprocity of the device is obeyed at all frequencies.

RTUIFR-18 1:30 PM

Ultra-Low Power RFIC Design Using Moderately Inverted MOSFETs: An Analytical/Experimental Study

A. Shameli, P. Heydari, University Of California at Irvine

This paper studies the use of moderately inverted MOS transistors in ultra-low power RFIC design. We introduce a new figure of merit for a MOS transistor, i.e., the gmfT-to-current ratio, which accounts for both the unity-gain frequency and current consuption during the optimization process of the transistor's performance. It is shown both experimentally and analytically that the gmfT/ID reaches its maximum value in moderate inversion region.

RTUIFR-19 1:30 PM

High Linearity Performance of 0.13um CMOS Devices using Field-Plate Technology

Chien-Cheng Wei, Hsien-Chin Chiu, and Wu-Shiung Feng, Department of Electronic Engineering, Chang Gung University, Taoyuan, Taiwan, R.O.C.

High linearity performance of 0.13um CMOS devices using field-plate technology is presented in this paper. The field-plate technology functions for reducing the electric field between the gate and the drain terminals, which provides a filed-plate induceddepletion region and decreased the leakage current to greatly improve the linearity and power performance of CMOS devices.

RTUIFR-20 1:30 PM

Wideband Lumped Element Model for On-Chip Interconnects on Lossy Silicon Substrate

S. Sun, R. Kumar, S. C. Rustagi, K. Mouthaan* and T. K. S. Wong**, Institute of Microelectronics,*National University of Singapore, **Nanyang Technological University.

This work presents the fully lumped element model for wideband on-chip interconnects, with large scalability of line lengths up to 8mm, and widths down to 100 nm. The equivalent lumped circuit is derived and verified to accurately recover the frequency-dpendent parameters up to 40 GHz, where all the parasitic effects are accounted for based on the EM simulation and measurement. Finally, the model is validated by comparing simulated and measured Scattering-parameters.

RTUIFR-21 1:30 PM

Systematic Design Methodology for On-Chip Transformers with Patterned Ground Shield

O. El-Gharniti, E. Kerhervé, J. B. Bégueret, IXL Laboratory at Talence, France

We present a systematic design procedure for on-chip transformers with patterned ground shield. The design procedure is based on transformers key geometrical parameters, on process technology specifications, and on a compact equivalent circuit model for n-chip transformers. The main aim is to provide designer with transformers with appropriate transformation ratio, optimum insertion loss at the targeted work frequency, and designated primary and secondary inductance values.

RTUIFR-22 1:30 PM

A Broadband and Scalable On-chip Inductor Model Appropriate for Operation Modes of Varying Substrate Resistivities

J. C. Guo, T. Y. Tan, Department of Electronics Engineering, National Chiao Tung University, Taiwan

A broadband and scalable model is developed to accurately simulate on-chip inductors of various dimensions and substrate resistivities. The broadband accuracy is proven over frequencies up to 20 GHz, even beyond resonance. A new scheme of RLC networks is deployed for spiral coils and substrate to account for 3D eddy current, substrate return path, and spiral coil to substrate coupling effects, etc. The 3D eddy current is identified as the key element essential to accurately simulate broadband characteristics. EM simulation using ADS momentum is conducted to predict the on-chip inductor performance corresponding to wide range of substrate resistivities (?Si=0.05~1KO-cm). Three operation modes such as TEM, slow-wave, and eddy current are reproduced. The model parameters manifest themselves physics-base through relevant correlation with ?Si over three operation modes. The onset of slow-wave mode can be consistently explained by a key element (RP) introduced in our model, which accounts for the conductor loss due to eddy current arising from magnetic field coupling through substrate return path. This broadband and scalable model is useful for RF circuit simulation. Besides, it can facilitate optimization design of on-chip inductors through physics-based model parameters relevant to varying substrate resistivities.

RTUIFR-23 1:30 PM

Minimization of Via Count in Multiple-Metal Inductors: Performance Characterization and Physical Modelling

Olive H. Murphy, Kevin G. McCarthy, Patrick J. Murphy, Department of Electrical and Electronic Engineering, , University College Cork, , College Road,, Cork,, Ireland.

High Q on-chip inductors are vital for modern RF ICs. A proven method of Q-enhancement is to use multiple metals stacked in a shunt manner, with a dense array of vias. The impact of fewer vias has not been investigated before. Here, we show that the sameQ can be achieved with significantly fewer vias, thus simplifying the inductor layout. The traditional and new approaches are explained and physical models developed which give excellent agreement between simulations and measurements up to 6GHz.

RTUIFR-24 1:30 PM

A 3GHz Subthreshold CMOS Low Noise Amplifier

Hanil Lee, Saeed Mohammadi, Purdue University

This paper presents an integrated 3GHz ultra low power CMOS LNA where MOS transistors are biased in subthreshold region. This LNA delivers a measured power gain of 4.5dB and noise figure of 6.3dB at only 160µW power consumption and 0.6V power supply. At 00µW, the LNA has a measured power gain of 9.1dB, a noise figure of 4.7dB, and IIP3 of -11dBm while S11 and S22 are less than -13dB. By using a Gain/Pdc ratio and an overall FOM, this LNA is superior to conventional published CMOS LNA designs.

RTUIFR-25 1:30 PM

An X-Band SiGe LNA with 1.36 dB Mean Noise Figure for Monolithic Phased Array Transmit/Receive Radar Modules

W.-M. L. Kuo, Q. Liang*, J. D. Cressler, M. A. Mitchell**, Georgia Institute of Technology, *IBM Microelectronics, **Georgia Tech Research Institute

This paper presents an X-band SiGe LNA for a monolithically integrated phased array T/R radar module. Implemented in a 200 GHz SiGe BiCMOS technology, the LNA occupies 730 ? 720 µm2, and dissipates 15 mW from a 2.5 V supply. The circuit exhibits a gain geater than 19 dB from 8.5 to 10.5 GHz, and a mean NF of 1.36 dB across X-band. At 10 GHz, the IP1-dB and IIP3 are -10.0 dBm and 0.8 dBm, respectively. To our knowledge, this LNA achieves the lowest NF of any LNA in Si-based technology at X-band.

RTUIFR-26 1:30 PM

A +7.9dBm IIP3 LNA for CDMA2000 in a 90nm Digital CMOS Process

D. L. Griffith, Texas Instruments, Inc.

A highly linear low noise amplifier has been implemented in a 90nm standard digital CMOS process. At 880MHz the amplifier provides an S21 of 14.5dB with a supply voltage of 1.4V and a current consumption of 8.3mA. The NF was measured to be 1.0dB and th input IP3 is +7.9dBm. Two lower gain modes have also been implemented; one with a lower transconductance gain stage, and one with a bypass switch. These performance parameters make the amplifier suited for the CDMA2000 cellular standard.

RTUIFR-27 1:30 PM

A 0.18µm RF CMOS Ultra Wide Band Transmitter Front End RFIC, Jun Zhao and Sanjay Raman, Bradley

Dept. of ECE, Virginia Tech, Blacksburg, VA, 24061, USA, email: sraman@vt.edu

This paper presents a 0.18?m RF CMOS Ultra wide band (UWB) transmitter front end RFIC for wireless sensor network applications. The proposed UWB transmitter is designed to generate a ~1.5 GHz bandwidth (-10dB) at center frequencies of 4 GHz or 8 GHz, in he form of 1ns gated wideband pulses with DBPSK/BPSK modulation. A novel pulse generator control circuit has been demonstrated to generate the desired 1ns pulses.

RTUIFR-28 1:30 PM

Low-Power Full-Band UWB Active Pulse Shaping Circuit Using 0.18-µm CMOS Technology

K.W. Wong, S. R. Karri, Y. Zheng , Institute of Microelectronics, Singapore

A low-power active pulse shaping circuit for UWB dual-band transmitter is presented. The circuit is fully integrated in 0.18-µm CMOS technology and only consumes a total power of 10.8mW from a supply voltage of 1.8V. It is composed of a passive part shapng the pulse and an active part providing gain over the whole UWB frequency range to fit the transmitted pulse to the federal communications commission mask. This output stage circuit provides a gain of 7 to 8dB across the band of interest.

RTUIFR-29 1:30PM

Frequency Characterization of a 2.4 GHz CMOS LNA by Thermal Measurements 443

D. Mateo, J. Altet, E. Aldrete-Vidrio, J. L. González, Universitat Politècnica de Catalunya, Electronic Engineering Department, Barcelona, Spain, Diego Mateo (mateo@eel.upc.edu), Jordi Girona 1-3, Edifici C-4, Universitat Politecnica de Catalunya, DEE", Barcelona, 08034, SPAIN

This paper presents a new technique to obtain electrical characteristics of analog and RF circuits, based on measuring temperature at the silicon surface close to the circuit under test. Experimental results validate the feasibility of the technique. Simulated results show how this technique can be used to measure the bandwidth and central frequency of a 2.4 GHz low noise amplifier (LNA) designed in a 0.35 microns standard CMOS technology.

RTUIFR-30 1:30PM

Optimization of PGS Pattern of Transformers/Inductors in Standard R BiCMOS Technology for RFIC Applications

H. B. Liang, Y. S Lin, C. C. Chen, J. H. Lee, National Chi Nan University

In this paper, a novel polysilicon PGS (Pattern Ground Shield) pattern, which located exactly inside and outside the spiral metal wires of the RF transformers/ inductors in standard RF BiCMOS technologoly, was demonstrated. The proposed PGS pattern can effectively improve the drawback, i.e. large parasitics between the transformers/inductors and the PGS pattern, due to no direct overlap between them. The results show a 56.5% (from 6.12 to 9.58) and a 55.7% (from 5.55 to 8.64) increase in Q factor, a 18.2 % (from 0.67 to 0.79) and a 21.4% (from 0.66 to 0.8) increase in GAmax, a 0.73 dB (from 1.74 dB to 1.01 dB) and a 0.85 dB (from 1.82 dB to 0.97 dB) decrease in NFmin, and a 18.4% (from 0.69 to 0.82) and a 21.2% (from 0.69 to 0.83) increase in magnetic-coupling factor kim were achieved at 4.2 and 5.2 GHz, respectively, for a bifilar transformer with an overall dimension 230 ◊ 215 µm2 in standard BiCMOS process with substrate thickness of 318 µm, and substrate resistance of 10 O∑cm. Furthermore, compared with the traditional PGS pattern, a 9.9% (from 10.1 GHz to 11.1 GHz) increase in resonant frequency fSR was achieved. These results means the proposed PGS pattern is very help for RF engineers to design high-performance RF transformers for ultra-low-voltage high-performance transformer-feedback LNAs and VCOs, and other RF-ICs which include transformers for SOC applications.

PANEL SESSIONS

Day	Time	Description
Mon	12:00pm - 1:20pm	4G: Do We Really Need 1 Gbits/s?
Tue	12:00pm - 1:20pm	SoC vs. SiP: Dollars & Sense
Wed	12:00pm - 1:20pm	Dueling Dualities: How to Best Marry Time-domain System-level Verification with Frequency-domain RF Circuit Simulations?
Wed	12:00pm - 1:20pm	RF PA Technology Roadmap for Wireless Infrastructure
Thu	12:00pm - 1:20pm	Delivering Winning Presentations: A Critical Skill for Engineers

RUMP SESSIONS

Day	Time	Description
Tue	6:00pm - 8:00pm	The Life of James Clerk Maxwell

RFIC SPONSORED PANEL SESSIONS (Details):

4G: DO WE REALLY NEED 1 GBITS/S?

Date & Time: Monday, June 12, 2006; 12:00pm - 1:20pm

Organizers: **Chris Rudell,** Intel
Yann Deval, IXL Lab
Stefan Heinen, RWTH Aachen University

Sponsor: MTT-23 RFIC

Panel: **Bernd Adler** , Infineon
David Ched, Spreadtrum
Barry Davis, Intel
Steve Lloyd, Beceem
Bill McFarland, Atheros

The RF community is currently running after high bit rates in wireless communications. Looking for hundreds of megabit per seconds large bandwidths are needed, while there is not that much available. Thus future applications are pushed towards higher frequencies. Specific modulation schemes are needed too which, in return, make the design of RF system more and more complex. But is the consumers' demand on high bit rate applications a reality? Is wireless communications at 1-gigabit-per-second a mass market requirement, or are there only a very few number of potential customers, making the effort to develop such applications a waste of time — and money? Are there that many phone users looking for high-resolution TV programs on a tiny screen, or do they just want to talk in their handset? Are we making things harder just for the fun of it? To answer these questions and others, panelists from semiconductor, data links and cell phone companies will present their views and will debate with the attendees.

SOC VS. SIP: DOLLARS & SENSE

Date & Time: Tuesday, June 13, 2006; 12:00pm - 1:20pm

Organizers: **Fazal Ali**, QUALCOMM
Mike Golio, HVVi

Sponsor: MTT-23 RFIC

Panel: **Bill Krenik**, Texas Instruments
Patrice Gamand, Philips
Andreia Cathelin, ST Microelectronic
Aravind Loke, Skyworks
Jeanne Pavio, Rockwell Collins
Participant, AMKOR

Recent years have seen dramatic miniaturization in the implementation of radio, microprocessor, memory and signal processing functions on mobile handsets. This increase in levels of integration is driven by the reduction in size, weight and cost as well as improvements in reliability realized in the resulting integrated radio. But these advantages are accompanied by engineering challenges related to all aspects of design, manufacturing and test.

Two distinct approaches: System on a Chip (SoC) and System in a Package (SiP) have evolved in addressing the mobile phone real-estate to support additional non-voice features.

The objective of this panel session is to compare the potential of each of these technologies to achieve size, weight and cost improvements.The participants will also discuss the relative merits and challenges these approaches offer in the area of design, manufacturing and test of integrated handset radios.

TUTORIALS

Day	Number	Time	Description
Sun	TSA	8:00am-5:00pm	Shrinking Passive Components – Dreams, Physics, Practical Design
Sun	TSC	8:00am-12:00pm	Introduction to UHF RFID: Readers, Tags and ICs
Sun	TSD	8:00am-5:00pm	Measurements Basics For Nonlinear HF Components
Mon	TMA	8:00am-5:00pm	High Speed Digital Signal Integrity
Mon	TMB	8:00am-5:00pm	Practical Methods for Determining the Accuracy of Measurements – A Review of Techniques Both Old and New
Mon	TMC	1:30pm-5:00pm	Introduction to MEMs Resonators and Filters
Fri	TFA	8:00am-12:00pm	Techniques of Frequency Synthesis
Fri	TFB	8:00am-5:00pm	Fundamentals of HF Through UHF Design
Fri	TFC	8:00am-12:00pm	Low-cost Microwave Photonic Component Technologies to Address Emerging Applications
Fri	TFD	8:00am-12:00pm	Ferrrite Devices for Low Frequency Applications
Fri	TFE	8:00am-12:00pm	Microwave and Millimeter-wave Packaging

SUNDAY TUTORIALS (Details):

These tutorials are targeted for people who are new to microwave design or new to specific technical areas. Each starts with basics to help you "impedance match" into the topic and help you understand papers on these topics later in Microwave Week.

TSA: CSHRINKING PASSIVE COMPONENTS – DREAMS, PHYSICS, P RACTICAL DESIGN

Date & Time: Sunday, June 11; 8:00 AM to 5:00 PM
Location: Moscone Convention Center, TBD

Topics & Speakers:

- CMOS Low Noise Amplifiers and Mixers, John Long, Delft University of Technology
- Design of CMOS Down-Conversion Mixers, Francesco Svelto, University of Pavia, Italy
- Frequency Synthesizers, Michael Perrott, Broadcom Inc.
- Receiver Architectures, Reza Rofougaran, Broadcom Inc.
- Polar CMOS Transmitters, John Groe, Sequoia Comm.
- Scaling CMOS to Microwave and mm-Wave Frequencies, Ali Niknejad, UC Berkeley
- Shrinking Passive Components – Dreams, Physics, Practical Design, Allen Podell, Consultant

Organizers: **Yann Deval**, University of Bordeaux, IXLlab
Sayfe Kiaei, Arizona State University
Bertan Bakkaloglu, Arizona State University, Connection One
Sponsor: MTT-23: RFIC

This workshop will focus on the development of RF CMOS Circuits for multi-GHz wireless applications. The workshop will focus on the design of fundamental building blocks encountered in RF transceivers including multi-mode receivers, receiver and transmitter blocks. Advantages and drawbacks of CMOS RF technologies are discussed. With the recent advances in sub-micron CMOS RF technologies, MOS transistors are capable of operating at RF and micro-wave frequencies of several GHz. RF CMOS offer several potential advantages relative to other technologies in terms of power, size, cost, and ease of manufacturing. However, there are constraints in RF CMOS in terms of noise, self gain, passive integration, isolation, etc.

WORKSHOPS

Day	Number	Time	Description
Sun	WSA	8:00am-5:00pm	Challenges of System Integration in Wireless and Nano-scale ERA
Sun	WSB	8:00am-5:00pm	RFICs for Ultra-wideband Systems
Sun	WSC	8:00am-5:00pm	Advanced Power Amplifier ICs for High Efficiency Mobile Transmitters
Sun	WSD	8:00am-5:00pm	Multi-chip Radio Module (MCRM) Design Methodology and Tools, and Manufacturing Issues for Cellular Appl.
Sun	WSE	8:00am-5:00pm	Noise Measurements and Modeling for CMOS
Sun	WSF	8:00am-12:00pm	Modeling Strategies for Silicon RFIC Intercomnnect: The Inclusion of Substrate Effects
Sun	WSG	1:30pm-5:00pm	Ultra Low Power Transceiver Design
Sun	WSH	1:30pm-5:00pm	Radio Transceivers for 3G/HSDPA and WiMAX User Equipment: System Architecture and Design Guidelines
Sun	WSI	8:00am-12:00pm	Three-dimensional Integration and Packaging
Sun	WSJ	8:00am-5:00pm	Advances in Multi-mode Multi-band Radio Transceivers
Sun	WSK	8:00am-5:00pm	Quality of Automotive RF Systems
Sun	WSL	8:00am-5:00pm	Memory Effects in Power Amplifiers
Sun	WSM	8:00am-5:00pm	Advances in GaN HEMT Device Technology, Modeling and Applications
Sun	WSN	1:30pm-5:00pm	NEW Advances in Oscillator Design
Sun	WSO	8:00am-5:00pm	SiBipolar and CMOS mm-wave ICs – From Process to Circuit Design and Applications
Mon	WMA	8:00am-5:00pm	UWB for Wireless Communicaions, Local Positioniing and Sensing
Mon	WMB	8:00am-5:00pm	Switching Mode Amplifiers with Applications to Wireless Transmitter Design
Mon	WMC	8:00am-12:00pm	Noise in SiGe and III-V HBTs and Circuites: Opportunities and Challenges
Mon	WMD	1:30pm-5:00pm	Passive and Active Differential Measurements: State-of-the-Art and Applications
Mon	WME	8:00am-5:00pm	Microweve Component Design Using Space Mapping Technology
Mon	WMF	1:30am-5:00pm	Active Antennas: Performance and Design
Mon	WMG	8:00am-5:00pm	Frequency Agile Radio: Systems and Technologies
Mon	WMH	8:00am-12:00pm	High Efficiency Power Amplifiers for Space and Terrestrial Applications

WORKSHOPS (continued):

Day	Number	Time	Description
Mon	WMI	8:00am-12:00pm	New CMOS Compatible Technologies for Enabling Cost-effective Base Stations in HFR Systems
Mon	WMJ	8:00am-12:00pm	Electronic Equalization Multigigabit Communications
Mon	WMK	8:00am-5:00pm	Practical RF and Microwave Multiplexer Design
Fri	WFA	8:00am-5:00pm	HIGH power Amplifier Reliability and Thermal Issues
Fri	WFB	8:00am-5:00pm	Technology and Applications of Wireless Sensor Networks
Fri	WFC	8:00am-5:00pm	New Optical Approaches of Wireless Sensor Networks
Fri	WFD	8:00am-5:00pm	How Accurate are Your THz Measurements?
Fri	WFE	8:00am-5:00pm	Advancing Methods for EM Computing

SUNDAY WORKSHOPS (Details):

WSA: CHALLENGES OF SYSTEM INTEGRATION IN WIRELESS AND NANO SCALE ERA

Date & Time: Sunday, June 11; 8:00 AM to 5:00 PM
Location: Moscone Convention Center, TBD

Topics & Speakers:
- Foundry Solutions for RF SoC Design, Albert Yen, UMC
- EDA Challenges for RF SoC Design, Scott Wedge, Synopsys
- Towards Manufacturability Closure for SoC Design, Charles Gore, Mentor Graphics
- Radios for Next Generation Wireless Networks, Reza Rofougaran, Broadcom
- Electrical Signal Integrity Analysis in Mixed-Signal and RF ICs, François Clement, CWS
- Theory of the Coupling Effects in SoC, G. Gielen, KUL
- Design Flow for Mixed Signal SoC and SiP Integration, François Lemery, STM
- A 60 GHz Wireless SoC in CMOS, Luiz Maria Franca Neto, Intel

Organizers: Yuhua Cheng, Siliconlinx Inc.
Didier Belot, ST Microelectronics
Jean Baptiste Begueret, IXL Laboratory
Sponsors: MTT-23: RFIC

As the semiconductor industry continually drives our life into 21st century with increased productivity and improved convenience throughout the economy, the IC industry is heavily investing in developing a technology platform for RF system integration in nano-scale and wireless era, in order to support the significantly increased demand for compact, low cost, and low power wireless products. Because both design and manufacturing technologies become much more complex in the nano-scale and RF world for RF system implementation, the challenges in designing and manufacturing chips with higher yields become much bigger than ever. These changes bring a new way of thinking in design and manufacturing. With a lot of fundamentals to be understood and a lot of technical barriers to be overcome, this workshop will bring the experts from foundries, EDA vendors and design companies to review the technology trends, challenges and opportunities in the development of an advanced platform technology for system implementation. A lot of details in advanced process technologies, device modeling, EDA design tools, design methodologies, system architecture and integration, packaging and testing will be addressed. The outcome will be greatly beneficial to the RF IC designers and technology platform developers in both industry and universities.

WSB: RFICS FOR ULTRA-WIDEBAND SYSTEMS

Date & Time: Sunday, June 11; 8:00 AM to 5:10 PM
Location: Moscone Convention Center, TBD

Topics & Speakers:
- Low Noise Receivers, Domine Leenaerts, Philips Res.
- Transmitter/Pulse Generator Circuits, Cam Ngyuen, Texas A&M
- Frequency Synthesizers for High Data UWB Systems, Edgar Sanchez-Sinencio, Texas A&M
- Distributed Circuits, Payam Heydari, UC Irvine
- RFICs for Position Location/RFID, Robert Wiegel, Tech. University Erlangen
- UWB Radar Sensor chipsets, Ian Gresham, M/A-COM
- UWB High-speed Personal Area Network System Standards and RFIC Design Implications, Roberto Aiello, Staccato

Organizers: **Sanjay Raman**, Virginia Tech., Electrical and Computer Engineering
A. Wang, Illinois Institute of Technology
Sponsors: MTT-23: RFIC

This workshop will focus on RFIC design and implementations for Ultra-wideband system applications, such as high-speed personal area networks, sensor networks, RFID, radar systems, etc. Topics will include low-noise receivers, transmitters/pulsegenerators, distributed circuits, baseband/signal-processing circuits, and system level issues for proposed UWB standards and other applications such as RFID and radar sensors. Particular attention will be focused on silicon-based IC implementations, and progress towards single-chip solutions. Attendees will be exposed to current issues facing RF/mixed-signal IC designers in the UWB space, and state-of-the-art IC implementations of UWB transmit, receive and back-end functions.

WSC: ADVANCED POWER AMPLIFIER ICS FOR HIGH EFFICIENCY MOBILE TRANSMITTERS

Date & Time: Sunday, June 11; 8:00 AM to 5:00 PM
Location: Moscone Convention Center, TBD

Topics & Speakers:
- Market Trends and Key Specifications of Cellular Transmitters, Eddie Spears and David Ngo, RFMD
- Market Trends and Key Specifications of Cellular, WLAN and WiMAX Transmitters, Ken Weller, Skyworks
- Polar Transmitter ICs for GSM/EDGE, Joe Staudinger, Freescale; Tirdad Sowlati, Skyworks; Alex Hietala, RFMD
- Amplifier ICs Using Analog Pre-distortion, Steve Kenney, Georgia Tech.
- Doherty and Vector Summing PA Techniques, Bob Stengel, Motorola
- PA Supply Modulation ICs, Larry Larson, UCSD
- Issues in Applying Digital Pre-distortion to Cellular Handset PAs, Claudio Rey, Freescale
- CMOS-based PAs, Ichiro Aoki and Scott Kee, Axiom Microdevices Inc.

Organizers: **N. Camilleri**, Alien Technology
J. Staudinger, Freescale
Sponsors: MTT-23 RFIC

Advancements in wireless transmitters have continued to focus on improving transmitter efficiency, at acceptable levels of linearity, while driving down both hardware cost and size. In addition, more spectrally efficient modulation techniques are being adopted to support the ever growing demands for high-speed data centric services. As such, it becomes ever more difficult to efficiently and cost-effectively amplify and transmit signals with wider instantaneous bandwidths and higher peak-to-average power ratios. This workshop will be both tutorial and advanced in nature. To begin, an overview of key transmitter requirements and specifications for a number of existing and emerging wireless systems will be reviewed. Secondly, a number of presentations will focus on some of the innovative developments occurring at the integrated circuit, system, and device technology levels. These include both stand-alone power amplifiers ICs, as well as more integrated transmitter architectures, and linearization systems. Selected examples will be presented for cellular and wireless data applications. Lastly, the intriguing possibility of implementing CMOS based power amplifiers will be examined.

WSD: MULTI-CHIP RADIO MODULE (MCRM) DESIGN METHODOLOGY AND TOOLS AND MANUFACTURING ISSUES FOR CELLULAR APPLICATIONS

Date & Time: Sunday, June 11; 8:00 AM to 5:00 PM
Location: Moscone Convention Center, TBD

Topics & Speakers:
- A Comprehensive Wireless Design Flow Enabling Design Productivity, J. Hartung, R.A. Mullen, Cadence
- Wireless System Simulation Using Agilent EDA Tools, Chris Mueth, Agilent Technologies
- Wireless Module Design: Multi-medium Concurrent Engineering of System, Circuit and Layout Using the AWR Design Environment, M. Heimlich, AWR
- Electromagnetic Simulation of Passive Components for RF Module Design Using Ansoft Simulation Tools Integrated to Layout, Matt Commens, Ansoft
- Precision Electromagnetic Analysis in a Multi-Chip Environment, Jim Rautio, Sonnet
- Successful Simulation Approaches for RF Module Design – Leveraging EM, SI, RF, SPICE and AMS Technologies in the Flow, Scott W. Wedge, Synopsys
- RF Module Design Methodology and Flow – Conception to Production, Checks and Balances, Jyoti Mondal, Morgan Fitzgibbon, Dermott Okeefe, Dan Saunders and Curt Hufford, Freescale Semiconductors
- Design and Verification for RF Systems Methodology, Flow and Simulation, Martin Barnasconi, Jan Niehof, Philips
- SiP Module Assembly for Cellular Application, Jaesun An, Jongho Han, ASE-Kr
- Challenge and Methodology for Cellular Applications, System and IC Co-Design, Kyutae Lim, Georgia Institute of Technology
- RF Module Assembly and Technology Integration, Eric Gongora, Stats Chippac
- Surface Finish and Maintaining 3 Sigma Design Tolerances on Critical Parameters for High Yield Radio Module Fabrication, Eric Lao, Unimicron
- Critical RF Module Assembly Rules, David Bolognia, AMKOR

Organizers: **Jyoti Prakash Mondal**, Freescale
Jan Niehof, Philips Research Lab
Didier Belot, ST Microelectronics
Sponsors: MTT-23 RFIC

MultiChip Radio Modules (MCRM) are becoming omnipresent parts in any handset for wireless and cellular applications. MCRM operates mostly in mixed signal environments and serves multiple functions. For example, an MCRM with DIGRF interface not only has transceiver function, it does the necessary control functions for power amplifier module as well as provides digital interface for the base band module. It saves space on board and lowers component counts. To customers, it is equivalent to lower cost and smaller size for cellular handsets. Presently three main modules (MCRM, PA and Base Band) cover all the necessary electrical functions in a cellular handset. Future MCRMs are likely to integrate more functions like PA. Designing low cost MCRM in ever shrinking size poses formidable challenges. Material properties and process tolerances need to be well defined. Keeping proper electrical isolation between various signals becomes quite messy. Tools to predict various coupling mechanisms need to be accurate. On top of it the modules need to be mechanically robust and RoHS compliant under various stress conditions. This also adds further constraint to the size and electrical performance of the module. This workshop will be divided into two sessions. The morning session will present a comprehensive tool set that is currently available to design MCRM. Goal is top system level module simulation with various chips inside. Not all the available tools will be discussed due to time constraint. Audience is welcome to discuss more. The afternoon session will have presentations from module design community, module substrate vendors, manufacturers and assembly houses; that will address various technology options (wire bond and flip chip), signal isolation issues, material properties, IC-substrate interface etc. Objective is to address the main issues and solutions for designing MCRMs, starting from design tools, SiP, SoC verification, design methodology to finished MCRM product. It is a vast topic. This workshop will capture at least some of the main challenges and proposed solutions.

WSE: NOISE MEASUREMENTS AND MODELING FOR CMOS

Date & Time: Sunday, June 11; 8:00 AM to 5:00 PM
Location: Moscone Convention Center, TBD

Topics & Speakers:

- Noise Parameter Characterization Techniques for CMOS Devices, Ali Boudiaf, Maury Microwave
- On-Wafer Noise-Parameter Measurement and Uncertainty Analysis at NIST, James Randa, NIST
- Alternative Parameter Sets and Insights into MOS Thermal Noise Behavior, Thomas McKay and G. Ali Rezvani, RF Micro Devices
- The Evolving Understanding of Noise Physics in Scaled Technologies and the Implications for Device Modeling and Data Interpretation, David Greenberg, IBM
- Modeling of RF Noise in MOSFETS with Industry Standard Models, James Victory, Jazz Semiconductor
- Modeling of Noise in Three Terminal Microwave Devices (FETs, HBTs) as Applied to CMOS Devices, Marian Pospieszalski, National Radio Astronomy Observatory
- RF Noise Characterization and Modeling of Deep-submicron CMOS, A.J. Scholten, Philips Research Laboratories Eindhoven
- RF Noise Modeling of MOSFETs Including Gate Current Effects, M. Jamal Deen, McMaster University

Organizers: **Jim Randa**, NIST
Tom McKay, RF Micro Devices
Sponsors: MTT-14 Microwave Low-Noise Techniques
MTT-11 Microwave Measurements
MTT-23 RFIC

CMOS technology, driven by a 30 years trend of increasing functionality of digital integrated circuits, continues to gain favor for an increasing range of low-noise radio-frequency applications. At the same time, noise figure continues to decrease with transistor gate length, challenging our ability to measure and extract intrinsic parameters. Moreover, future devices may bring into play new physical effects with unforeseen impact, increasing the need for characterization methods relying on few assumptions, valid at the specific frequencies of interest. This workshop will cover the current status and challenges in the measurement and modeling of the noise properties of CMOS devices, particularly at frequencies in the low microwave range. We will review present noise-parameter measurement methods, their capabilities, and their limitations for CMOS transistors. The modeling implications of measurement data will be discussed, along with possible new directions in relating noise measurements to models. Different approaches to the modeling of the noise properties of these devices will be presented, as will methods for the extraction of model parameters from measurement data. It is hoped that the workshop will stimulate and provide a basis for further improvements in the measurement and modeling of noise in CMOS devices, particularly at frequencies around 1–10 GHz.

WSF: SUBSTRATE EFFECTS IN SI RFIC INTERCONNECT

Date & Time: Sunday, June 11; 8:00 AM to 12:00 PM
Location: Moscone Convention Center, TBD

Topics & Speakers:

- Physical Considerations in Modeling Interconnect Near Silicon Substrate, J. Dunn, Applied Wave Research
- Modeling of Interconnects and Spiral Inductors in Silicon RFICs, A. Weisshaar, Oregon State University
- Simulation and Modeling Strategies in a Silicon World, B. Brim, Ansoft Corp.
- Simulation and Modeling of Substrate Coupling, M. Steer, North Carolina State University
- RF CMOS Design – Living with the Substrate, D. Allstot, University of Washington

Organizers: **J. Dunn**, Applied Wave Research
Sponsors: MTT-23 RFIC

Silicon RFIC technology normally requires that there be a lossy silicon substrate. Substrate effects make it more difficult to develop accurate passive component and interconnect models. The substrate creates a number of problems for the designer: eddy current losses, coupling between digital and analog blocks, poorly defined signal path return and ground. In this workshop, we will examine how substrate issues are being addressed by CAD support modeling experts and high speed IC design engineers. Time is allocated for attendees to share their own insights and experiences.

WSG: ULTRA LOW POWER TRANSCEIVER DESIGN

Date & Time: Sunday, June 11; 1:30 PM to 5:00 PM
Location: Moscone Convention Center, TBD

Topics & Speakers:

- Ultra Low-Power Radio Design for Wireless Sensor Networks, Christian C. Enz, Swiss Federal Institute of Technology
- Low Power Frequency Synthesizers Architectures, Franck Badets, ST-Microelectronics
- Ultra-Low Power ZIGBEE Transceivers, Shahin Farahani, Freescale Inc.
- Low Power Ultra-wideband Transceivers, Hossien Hashemi, University of Southern California
- Low Power Transmit Architectures, Bertan Bakkaloglu, Shahin Talei, Sayfe Kiaei, Connection One

Organizers: **Sayfe Kiaei**, Arizona State University
Yann Deval, University of Bordeaux, IXLlab
Sponsors: MTT-23 RFIC

This workshop will address design and development of ultra-low power transceiver systems. The workshop will focus on several key low power systems and will examine the tradeoffs among these transceiver: Wirenet, ZIGBEE, and Ultra-Wide Band Transceivers. The market of low power, low data rate RF sensors and RF networks is growing fast. These networks require ultra low power transceivers and the battery life is critical in these systems. The workshop will address design methodologies and advanced technologies dedicated to the design of low power transceivers, based on practical examples, for the attendees to be able to develop their own products at the end.

WSH

RADIO TRANSCEIVERS FOR 3G/HSDPA and WiMAX USER EQUIPMENT: SYSTEM ARCHITECTURES AND DESIGN CHALLENGES

Date & Time:
Location:

Topics & Speakers:

1. 802.16e WiMAX Key System and Circuit Design Issues, **S. Llyod and L. Jalloul**, *Beceem Communications, Inc.*
2. 3G/HSDPA Radio Transceiver Chipset: Design Issues and Challenges, **A. Bellaouar**, *Sirific Wireless Corp.*
3. RF System Issues and RF Impairments Compensation in WiMAX Radios, **D. Schmidt**, *Intel Co.*
4. PA Linearization Techniques and Design Issues for WiMAX OFDM-based Applications, **D. Kimball**, *UC San Diego*
5. Transceiver architectures and RF Impairments Compensation in Future 3G/HSDPA Radios, **W. Ali-Ahmad**, *AUB*

Organizers:
W. Ali-Ahmad, *AUB*

Sponsors: MTT-23, RFIC Symposium

As we move into the era of merged fixed and mobile wireless broadband networks, two standards are competing to service that huge market: 3GPP/HSDPA and WiMAX 802.16d/e. Many established and start-up companies are already working on developing radio chipsets and user equipment to handle the future market demand for mobile wireless broadband systems. These wideband and mobile systems impose tough performance requirements on the radio in order to maintain a high Quality-of-Service (QoS). This half-day workshop will present and discuss the different radio chipset architectures, key system issues, and circuit design challenges, related to the design of 3G/HSDPA and WiMAX radio transceiver chipsets. In addition, the workshop will stress on the importance of use of baseband DSP compensation of RF system impairments in these future broadband applications.

WSJ: ADVANCES IN MULTI-MODE MULTI-BAND RADIO TRANSCEIVERS

Date & Time:: Sunday, June 11; 8:00 PM to 5:00 PM
Location: Moscone Convention Center, TBD

Topics & Speakers:

- System Requirements for Multi-mode Multi-band Transceivers, E. Niehenke, Niehenke Consulting
- Semiconductor Technology Considerations for Implementing RFIC Transceivers, T. O'Connell, IBM Systems and Technology Group
- Is Direct Conversion the Answer?, E. Nash, Analog Devices
- All-Digital Frequency Synthesizer-based Transmitter and Direct-Sampling Receiver for Mobile Phones, B. Staszewski, Texas Instruments Inc.
- Multi-Standard RFIC Transmitter Technology, L. Larson, UCSD Center for Wireless Communications
- Reconfigurable CMOS Digital TX Architectures for Cellular and Connectivity Applications, A. Pozsgay, ST Microelectronics Inc.
- Challenges in Future Multiradio Transmitters, E. Järvinen, Nokia Corp.
- Software Radio Receiver Design, R. Hinkling, TechnoConcepts Inc.
- Diversity Receivers for Multi-mode Handsets, K. Sahota, P. Gudem, Qualcomm Inc.
- Multi-Mode Polar Transmitters, John Groe, Sequoia Communications

Organizers: **E. Niehenke**, Niehenke Consulting
U. Dhaliwal, ST Microelectronics Inc.
S. Heinen, RWTH Aachen University
Sponsors: MTT-6 Microwave and Millimeter-Wave Integrated Circuits
MTT-20 Wireless Communications
MTT-23 RFIC

There is a gradual evolution toward integration of multifunction, multistandards in radio transceivers for wireless communications. Minimizing part count and cost is paramount. There are planned future services and evolved products, which contain both Cellular Communication and Wireless Connectivity features with Global and Nomadic roaming for voice and data. This workshop will first address the key requirements for each system. The suitability of the different transmitter and receiver types will be considered for the various systems highlighting their strong and weak points. Techniques to generate an all-digital transmitter frequency synthesizer, as well digital receiver reception will be reported. The goal is to find common transceiver architectures that are flexible whilst meeting the requirements of such systems. Recent advances in semiconductors, transceiver architecture, and state-of-the-art designs will be presented. Performance of each design will be highlighted with techniques to overcome their possible weak points.

WSO: SI BIPOLAR AND CMOS MM-WAVE ICS – FROM PROCESS TO CIRCUIT DESIGN AND APPLICATIONS

Date & Time: Sunday, June 11; 8:00 AM to 5:00 PM
Location: Moscone Convention Center, TBD

Topics & Speakers:

- Millimeter Wave ICs for System Applications: Design Methodology and Challenges, Debabani Choudhury, Intel
- From Transmission Lines to Transceivers: Silicon Millimeter-wave ICs for 60 GHz and Beyond, Brian A. Floyd, IBM
- SiGe BiCMOS mm-wave SoC Transceiver Design, Noyan Kinayman, M/A-COM Strategic Res. and Dev.
- Design Techniques in Millimeter-wave Range Using Conventional SiGeC BiCMOS Technology, Sebastien Pruvost, STMicroelectronics
- Extending RF-CMOS to mm-wave Applications, John J. Pekarik, IBM Semiconductor Res. and Dev. Ctr.
- Perspectives of Downscaled CMOS for RFIC and mm-wave Applications, Stefaan Decoutere, IMEC, Belgium
- 0–60 GHz in Three Years: mm-Wave CMOS Research at BWRC, Ali M. Niknejad, UC at Berkeley, CA
- Analog Integrated Circuits on VLSI SOI CMOS for High-Speed Wireless Communication up to 60 GHz, Frank Ellinger, ETH/IBM, Electronics Lab.
- Design Techniques for mm-wave CMOS Circuits, Herbert Zirath, Charlmers University of Technology
- CMOS mm-wave IC Designs: VCOs and Amplifiers, Huei Wang, National Taiwan University

Organizers: **Hiroshi Kondoh**, Hitachi Central Res Lab.
Luciano Boglione, IECi
Sponsors: MTT-23: RFIC
MTT-6 Microwave and Millimeter-Wave ICs
IMS2006

This workshop will concentrate on the efforts currently under way in the mm-wave arena to enable silicon-based applications. The potential advantages of the silicon technology are obvious: more integration and lower costs. However, the challenges that silicon brings about cannot be underestimated: circuit designers must develop new skills to cope with a lossy substrate coupled with intrinsic device limitations. While the SiGe bipolar device is emerging as a feasible solution to the design of mm-wave circuits, pure CMOS solutions are also being considered as commercial 0.13 and 0.09 mm CMOS processes are paving the way to even more exciting opportunities. This full day workshop will be structured in 2 parts: Part I will focus on SiGe bipolar designs with the intent of discussing the technical and practical challenges that designers face in the mm-wave range as they reach higher and higher frequencies of operation. Part II will look into the current and future status of pure CMOS technologies and review the related state-of-the-art results. The business challenges related to mm-wave applications will also be considered during these presentations.

REGISTRATION

REGISTRATION REQUIREMENTS

Registration fees are required of all participants, including session chairs, authors, workshop and panel session organizers and speakers.

ADVANCE REGISTRATION

All registrants who select the IEEE member rates will be required to produce their current IEEE membership cards upon check-in at the conference. Registrants who do not have their current IEEE membership cards at check-in will be charged nonmember rates.

Reduced rates are offered for advance registration when received by May 5, 2006. A registration form is available as an insert to this program. Each registrant must submit a separate form, with payment, to the address shown at the bottom of the registration form. If using a credit card, then fax and online registration is available. When mailing, please mail early to ensure receipt by the deadline; otherwise, on-site fees will apply.

Individual remittance must accompany the registration form and is payable in US dollars only, using personal check drawn on a US bank, traveler's check, international money order or credit card (MasterCard, VISA or American Express) are accepted. Personal checks must be encoded at the bottom with the bank number, account number and check number. Bank drafts, wire transfers and cash are unacceptable and will be returned. Government or company purchase orders will not be accepted and will be returned.

GUEST REGISTRATIONS

To preregister your guest, include his or her name on your advance registration form. Guest badges will be included in the envelope that you will receive upon check-in. Onsite guest registration also will be available.

STUDENTS, RETIREES AND LIFE MEMBERS

Students, retirees and IEEE Life Members receive a substantial discount on the IMS registration fee. CD ROMS are not included. To qualify as a student, a registrant must be either a student member of IEEE or a full-time student carrying a course load of at least nine credit hours. ARFTG also provides discounts for students and retirees.

PRESS REGISTRATION

Credentialed press representatives are welcome to register on-site only, at the Exhibitor Counter, without cost.and thereby have access to technical sessions and exhibits. Digests are not included. The Press Room is located in Room 304.

ON-SITE REGISTRATION

On-site registration for all Microwave Week events will be available at the Moscone Convention Center. Registration hours are:

Saturday, June 10	2:00pm - 6:00pm
Sunday, June 11	7:00am - 6:00pm
Monday, June 12	7:00am - 5:00pm
Tuesday, June 13	7:00am - 5:00pm
Wednesday, June 14	7:00am - 5:00pm
Thursday, June 15	7:00am - 3:00pm
Friday, June 16	7:00am - 9:00am

ON-SITE REGISTRATION FEES	IEEE Member	Non-Member
Int'l Microwave Symposium		
All IMS Sessions	$480	$720
(Includes Exhibits, Abstract Book and IMS CD ROM)		
All IMS Sessions	$415	$610
(Includes Exhibits, Abstract Book no IMS CD ROM)		
Single Day	$250	$350
(Includes Exhibits, Abstract Book and IMS CD ROM)		
Student, Retiree, Life Member	$75	$150
(Includes Exhibits, Abstract Book and IMS CD ROM)		
RFIC SYMPOSIUM (Mon. & Tue.)	$250	$360
(Includes Exhibits, RFIC Sessions & Reception, RFIC Digest and CD ROM)		
RFIC Reception Only	$60	$80
ARFTG Conference (Fri.)		
(Includes Exhibits, Breakfast, Lunch, Digest and ARFTG Exhibition. Member rates available to ARFTG or IEEE members.)		
ARFTG Conference	$235	$365
ARFTG Student, Retiree	$150	$150
Additional Digests and CD ROMs *(on-site pickup only)*		
IMS and ARFTG CD ROM	$65	$130
RFIC Digest	$75	$90
RFIC CD ROM	$65	$130
ARFTG Digest	$60	$85
ARFTG Archive CD-ROM	$65	$90
Optional Box Lunches for Panel Sessions	$25	$25
Awards Banquet *(Wed. Evening)*	$70	$90
Exhibits Only	$20	$20
Guest Programs		
IMS2006 Golf Tournament		$85.00

For all other guest program registrants go to www.signaturesf.com/ieee

Workshops/ Tutorials	IEEE Member	Non Member	Student/Retiree Life Member
Full Day	$200	$300	$135
Half Day	$150	$225	$100
All Workshop CD plus 1 workshop	$440	$650	$250

REFUND POLICY

Written requests received by May 5, 2006 will be honored. **Refund requests postmarked after this date and on-site refunds will be granted ONLY if an event is cancelled.** This policy applies to registrations for the symposium sessions, workshops, tutorials, digests, extra CD-ROMS, panel sessions, awards banquet and guest programs. Please state the pre-registrant's name and provide a mailing address for the refund check; if registration was paid by credit card, refund will be made through an account credit. Account number must be provided if the initial registration was done on-line. Address your requests to: MTT-S Registration, 685 Canton St., Norwood, MA 02062.

GENERAL INFORMATION

Information Booth: Pamphlets and information on the San Francisco area will be available at a booth centrally located in the registration area of the convention center. The hospitality suite is located in the Marriott Hotel. Sign in and guest badges will be required to insure exclusive guest use.

IEEE/MTT-S Memberships: Those who apply for IEEE membership before registering for the Symposium will be eligible for IEEE member discounted registration fees. Membership applications and payments will be accepted at the IEEE Booth in the registration area. IEEE members (or on site applicants) who register for the full Symposium and have not been MTT-S members in the past year will be offered a free basic MTT-S membership, good until the end of the year.

Children: Children under the age of 14 will not be admitted to the exhibition hall at any time.

Drinks and Refreshments: Free coffee and soft drinks will be available during midmorning and midafternoon breaks in the refreshment areas in the exhibition hall.

Smoking: Smoking is not permitted in the MCC. All restaurants and bars in San Francisco are 100% smoke-free, but if there is outdoor seating, smoking is allowed outdoors. Most hotel rooms are also designated as smoke free. If you are a smoker, it is suggested that you register for your hotel early to ensure a smoking room is available. Stiff penalties are applied for smoking in non-smoking rooms.

Recruiting: Businesses do not send their personnel to the IMS to be recruited by the other businesses. To ensure that good attendance to these meetings continues in the future, IEEE policy insists that recruiting does not occur at the Symposium.

Recording of Technical Presentations: The recording of technical presentations by video or audio recorders or cameras is not allowed without the permission of the speaker and notification of the session organizer.

VISA INFORMATION: TEMPORARY VISITORS TO THE US
International travelers (citizens of other countries) coming to US temporarily require a VISA to enter the US that relates to the purpose of their travel. Please contact your local American Embassy or Consulate as early as possible to determine if you need a Visa to enter the US. To avoid frustrations and disappointments, please contact your local American Embassy or Consulate for information about current visa processing time estimates and processes. You can also contact the US embassy or consulate via the US Department of State site at http://travel.state.gov/visa/tempvisitors_info Please apply for your visa as early as possible. Visa applications are now subject to a greater scrutiny than in the past. For many applicants, a personal appearance interview is required as a standard part of visa processing. This can cause longer processing times since applicants affected by these procedures only get informed of the need for additional screening at the time they submit their applications. Citizens of certain countries may be able to travel on a Visa Waiver Program (VWP) if they meet certain conditions. Participating Countries in the VWP include Andorra, Australia, Austria, Belgium, Brunei, Denmark, Finland, France, Germany, Iceland, Ireland, Italy, Japan, Liechtenstein, Luxembourg, Monaco, the Netherlands, New Zealand, Norway, Portugal, San Marino, Singapore, Slovenia, Spain, Sweden, Switzerland and United Kingdom. Starting October 1, 2003, each Visa Waiver Program traveler must present a machine-readable passport (MRP) at the US port of entry to enter the US without a visa. Otherwise a nonimmigrant visa is required. Additional information can be found on the US Department of State Bureau of Consular Affairs Visa Services Web site at http:// travel.state.gov/nonimmigrantvisas.html

SOCIAL EVENTS

RFIC SYMPOSIUM RECEPTION: Sunday evening, June 11, is a highlight of RFIC technical activity and social events. The evening begins with the official opening of the technical program at the RFIC Plenary session at 5:30 PM in the SFCC Esplanade Ballroom. All attendees and their spouse (or guest) are invited to the RFIC Reception which immediately follows the Plenary session at 7:00 PM. Tickets for the Reception will be found in the attendees registration packet. Additional tickets may be purchased at the Symposium registration.

MICROWAVE JOURNAL/MTT-S RECEPTION: All Microwave week attendees and exhibitors are invited to attend a reception hosted by Microwave Journal and MTT-S on Monday, June 12 from 5:30 to 7:30 PM at the Yerba Buena Gardens, just across the street from the Convention Center and the Marriott.

IEEE MTT WOMEN IN ENGINEERING RECEPTION: The IEEE MTT WIE committee will host a meeting and reception on Tuesday, June 13, 5:30–7:00 PM, at the Marriott Hotel. HAM RADIO RECEPTION: All radio amateurs who are attending IMS 2006 are invited to a social gathering on Tuesday, June 13, 6:00–9:00 PM, at the Marriott Hotel.

STUDENT RECEPTION: A reception for all students will be held at the Marriott Hotel on Tuesday, June 13 before the Maxwell Rump sessions. All students are invited to attend. MAXWELL RUMP SESSION RECEPTION: A reception will be held for all attendees of the Maxwell rump session prior to the presentation at the Marriott Hotel. INDUSTRY HOSTED COCKTAIL

RECEPTION: Symposium exhibitors will host a cocktail reception on Wednesday, June 14, from 5:45 PM to 7:15 PM at the Marriott. Complimentary beverage tickets will be included in the registration packages.

IEEE MTT-S AWARDS BANQUET: The annual Awards Banquet will be held on Wednesday, June 14, from 7:30 PM to 10:00 PM at the Marriott Hotel. The evening will include a fine dinner, awards presentation and entertainment. Major society awards will be presented at this event. The banquet is free of charge for the awardees.

IEEE MTT-S STUDENT AWARDS LUNCHEON: Student Paper Awards, MTT graduate Fellowships and MTT undergraduate scholarships will be presented at the Student awards luncheon at noon on Thursday, June 15 at the Marriott Hotel. The Luncheon is free for all student paper finalists and their advisors.TECHNICAL ATTENDEES BREAKFAST: Monday–Thursday at the convention center lobby from 7:00 AM to 9:00 AM. This breakfast is for all persons registered as technical participants in the IMS, RFIC or ARFTG. Badge required for admission.

TRANSPORTATION

The City of San Francisco is located on the northern tip of the peninsula created by the Pacific Ocean to the west and the San Francisco Bay to the east. This geography determines the locations of the major roads and transit systems. San Francisco is connected to San Jose by US Highway 101 which runs south along the west side of the bay and also by Interstate 280 which runs south along the spine of the peninsula hills. San Francisco is connected to Oakland by Interstate 80 over the Bay Bridge and by Interstate 880 which runs along the east side of the bay. San Francisco is served by the Muni Transit System in San Francisco, BART Transit System to San Francisco Airport and Oakland Airport, and CALTRAIN to San Jose. Downtown San Francisco is easy to get around via the Muni transit system, taxi, or walking. The convenience of having a car in the City of San Francisco may be reduced by the limited availability of parking and its expense. There are three nearby airports hosting all major domestic and international air carriers in the Bay Area. San Francisco International Airport is the most conveniently located and offers a greater variety of flights. However, it may have higher airfares and may be subject to flight delays during periods of low clouds. Oakland International Airport and Norman Y. Mineta San Jose International Airport may have lower airfares and may be less subject to delays.

San Francisco International Airport (airport code SFO): The Moscone Center and conference hotels are located just 13 miles by ground transportation from the San Francisco Airport. The BART link http://www.bart.gov/guide/airport/sfo.asp compares available ground transportation and their estimated costs:

Destination

Downtown SF
Taxi: $25–$37
Shuttle Van: $12–$17
Daily Car Rental: $39–80
BART: $4.95

GUEST PROGRAM

All tours have a 30 guest minimum with the exception of Muir Woods. If the tour minimum is not met 14 business days prior to the scheduled tour date, the tour will be subject to cancellation. All tour fees will be completely refunded to the IEEE attendee in the event of a tour cancellation. All tours depart from The San Francisco Marriott's Mission Street exit. Look for a uniformed tour guide wearing black with a sign listing your tour. The guide will be stationed in the Marriott lobby. A Signature Hospitality Group representative will be available daily in the Hospitality Suite.

Additional tour information can be found at:
www.signaturesf.com/ieee
Tour pricing and latest updates are found here.
Guest tickets are available only through this website.

Sunday, June 11, 2006 — Muir Woods, Sausalito & Golden Gate Bridge
Hours: 12:00 PM–4:00 PM
The Marin Headlands, perched above the spires of the Golden Gate Bridge, is a geographically unique vantage point where, high above the city, guests will enjoy one of the area's best and most beloved city and ocean vistas. Continuing north, guests will stop in Muir Woods, a spot described by conservationist John Muir as "the best tree-lovers monument that could possibly be found in all the forests of the world."

Monday, June 12, 2006 IMS2006 — Golf Tournament
Hours: 8:00 AM (Players must register by 8:00 AM
Presidio Golf Course, 300 Finley Rd., San Francisco, CA Play: Staggered Tee times, "Scramble" rules for each Team of 4 Players

Monday, June 12, 2006 — Alcatraz, Fisherman's Wharf & Pier 39
Hours: 10:00 AM–2:00 PM
Includes: Roundtrip motor coach transportation Professional tour guide throughout the day Ferry & admission to Alcatraz Free time at Fisherman's Wharf and Pier 39 All applicable taxes, fees and gratuities

Tuesday, June 13, 2006 — Walking Tour of Chinatown
Hours: 10:00 AM–2:00 PM
Includes: Detailed walking tour of Chinatown by a Neighborhood Native Tour Guide Free time for shopping & lunch Visit to temples, markets and a Fortune Cookie factory All applicable taxes, fees and gratuities

Tuesday, June 13, 2006 — San Francisco City Tour
Hours: 10:00 AM–2:00 PM
Includes: Roundtrip motorized cable car transportation Tour of San Francisco highlights Photo stops at several San Francisco attractions Free time for lunch Professional Tour Guide on cable car throughout the tour All applicable taxes, fees and gratuities

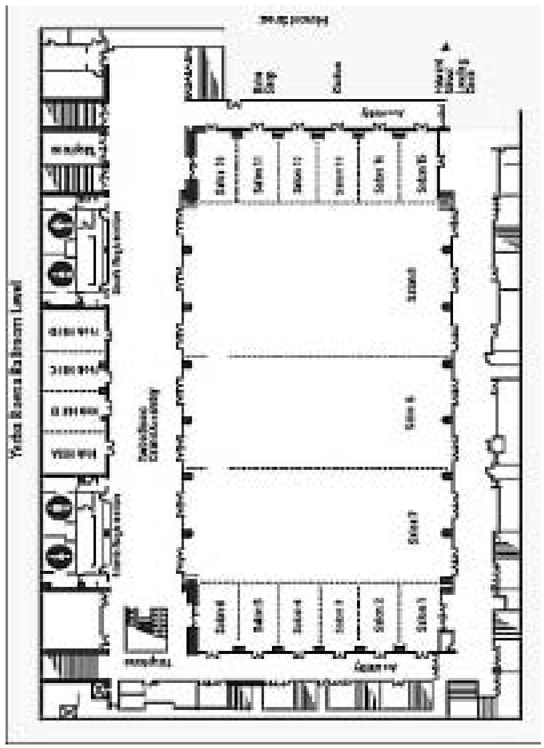
Wednesday, June 14, 2006 — Golden Gate Park, Japanese Tea GARDENS & New de Young Museum
Hours: 10:00 AM–2:00 PM
Includes: Roundtrip motor coach transportation Guided tour of the Golden Gate Park Highlights Admission for de Young Museum Admission fees for the Japanese Tea Gardens & Conservatory of Flowers All applicable taxes, fees and gratuities

Thursday, June 15, 2006 — Monterey, Carmel & Pebble Beach
Hours: 10:00 AM–6:00 PM
Includes: Roundtrip motor coach transportation Entrance to 17-Mile Drive Free time in Monterey and Carmel for shopping & lunch Professional tour guide throughout the day All applicable taxes, fees and gratuities

Thursday, June 15, 2006 — Wine Country Tour
Hours: 10:00 AM–5:00 PM
Includes: Deluxe motor coach transportation Tour and tasting at three wineries Free time for lunch & picnicking Professional tour guide throughout the day All applicable taxes, fees and gratuities

Friday, June 16, 2006 — Yosemite National Park
Hours: 7:00 AM–9:00 PM
Includes: Roundtrip motor coach transportation to Yosemite National Park Free time for lunch Snacks and bottled water Professional tour guide throughout the day All applicable taxes, fees and gratuities

Marriott Floor Plan



Moscone Exhibit Halls